CMOS NAND Gate Circuit

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Abstract

The term Cmos stands for Complementary Metal Oxide Semiconductor. This technology makes use of both P channel and N channel semiconductor devices. Real world signals are mostly based on Boolean Operators. Boolean Operators are simple words AND, OR, NOT or AND NOT used as conjunctions to combine or exclude keywords in a search, resulting in more focused and productive results. There are various basic gates which are extensively used in the designing of the more complex circuits with higher number of transistors. The NAND or Not AND function is a combination of the two separate logical functions, the AND function and the NOT function connected together in series.

1 Circuit Details

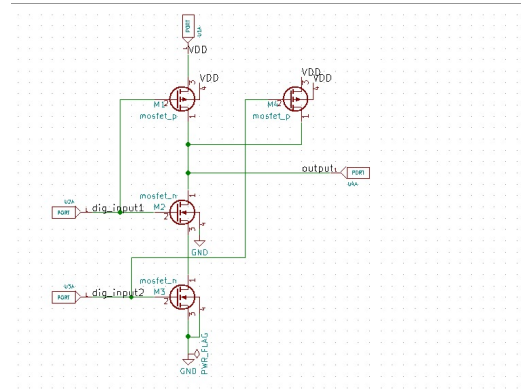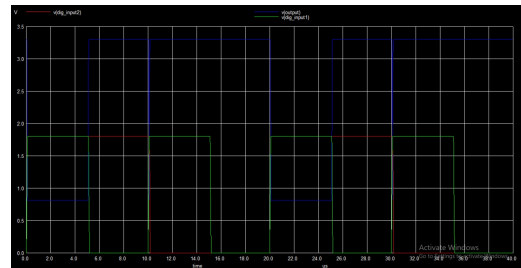The NAND or Not AND function is a combination of the two separate logical functions, the AND function and the NOT function connected together in series.Considering the truth table,Case 1 When A=B=0,both the NMOS are in OFF condition and PMOS are in ON condition. Therefore the output is connected to VDD 1.8 v and 1.1 v HIGH logic is present at the output terminal. Case 2 When A=0 and B=1, the upper NMOS are in OFF and lower NMOS in ON condition. Left PMOS are in ON and right PMOS in OFF condition. Therefore the output is connected to VDD and HIGH logic is present at the output terminal. Case 3 When A=1 and B=0, upper NMOS are in ON and lower NMOS in OFF condition. Left PMOS are in OFF and right PMOS in ON condition. Therefore the output is connected to VDD and HIGH logic is present at the output terminal. Case 4 When A=B=1,both the NMOS are in ON condition and PMOS are in OFF condition. Therefore the output is connected to VDD and LOW logic is present at the output terminal. Power consumption plays an important role and it affects proportionally to the performance of the circuit. The duplication and scaling means adding of transistors i.e connecting transistor in parallel or series to NAND gate. The duplication and scaling means adding of transistors i.e connecting transistor in parallel or series to NAND gate. The high level approach for estimating circuit reliability tends to consider the probability of failure of a logic gate as a constant, and work towards the higher levels.

2 Implemented Circuit

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

Figure 2: Implemented waveform.

References

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[3] P. S. Wankhede. Design and analysis of nand gate using 180nm and 90nm cmos technology. https://www.academia.edu/34819983/Design_and_Analysis_of_NAN