A D-Type Flip-Flop with Enhanced Timing Using Low Supply voltage.

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Abstract

This work proposes a novel master-slave latch D type FlipFlop.The proposed flip-flop is built from 22 transistors design with only 6 transistors in the clock network.It consists of a reset-set slave latch and an asymmetrical single data input master latch.By reducing the number of stages in master latch setup time has been significantly reduced and power consumption has improved.The proposed flip-flop is competitive to other state of the low power flip-flops by reducing the power consumption and area.Flip-Flops are digital circuits used in modern integrated circuits to control the flow of data using a specified clock.This circuit can be used in Counters and Registers.

1 Circuit Details

FlipFlops are widely used in Very Large-Scale Integrated circuits-VLSI.They are considered fundamental building blocks in sequential circuits like memories for data storage, and registers for data transmission.There are many parameters that specify the flop's performance like setup and hold times CLK to Q delay time, layout area, power dissipation and leakage current.The master latch consists of two stages with one input D. The master latch X1 and X2 outputs are taken from two series stages to be used as inputs to reset-set slave latch. The feedback in the master latch is a weak back-to-back inverter in order not to adversely impact the data propagation. When CLK is low the data can pass its value to X1 and X2 nodes in the master latch. While in the slave latch PCK transistor is ON. This enables the back-toback feedback inverters P5/N5 and P6/N6 which hold X4 and X5 values stored from previous state. Once CLK changes its value to high passing new D value to X1 and X2 is disabled and the old X1 and X2 values are maintained using PF1/NF1 weak feedback inverter. On the other hand the slave latch will be enabled the new values of X1 and X2 are loaded into the slave latch and the updated value of X4 will pass to the output.The master latch implementation in the proposed design has improved the setup time. Also, the proposed design has shown that it has faster CLK-Q propagation time and less power consumption.

2 Implemented Circuit

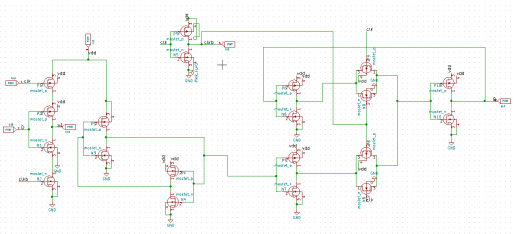

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

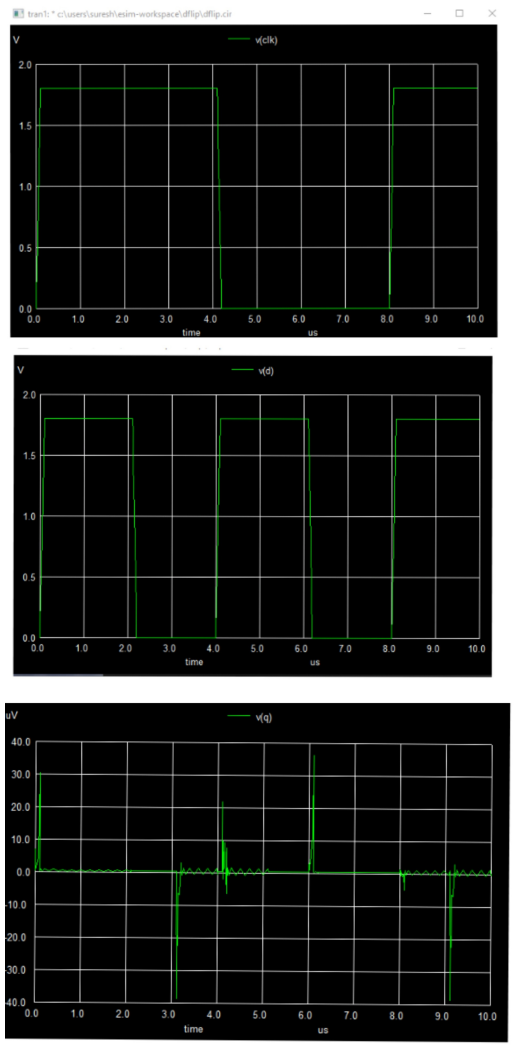

Figure 2: Implemented waveform.

References

[1] . J. S. L. Geng and C. Xu. Design of flip-flops with clock-gating and pull-up control scheme for power-constrained and speed-insensitive applications. IET Computers & Digital Techniques., vol. 10, no. 4, pp. 193–201, July. 2016.

[2] S. J. N. K. Y. I. K. A. H. S. N.Kawai and Y. Tanaka. A fully static topologically-compressed 21-transistor flip-flop with 75. IEEE J. Solid-State Circuits, vol. 44, no. 11, pp. 2526–2533, Nov. 2014.