Multiplexer based design of Half Adder

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Abstract

Low power design is the decisive factor for designing a circuit. The designed circuit is a high speed, high performance 1- bit half adder circuit using multiplexer which has applications in ASIC and ALU(arithmetic logic unit). MUX is a universal logic and can be used to design all logic gates. MUX is used to reduce the number of IC packages in a given circuit. This in order reduces the area , propagating delay and power dissipation. Half Adder is a combinational circuit which adds two binary digits, it is the base of many functional operations Example : subtraction ,multiplication ,division ,a full adder can be designed using half adder circuitry and is a major functional block in ripple carry adder.

1 Circuit Details

Half Adder is used to add two 1 bit numbers. It has two binary digit inputs (A and B) , two outputs(S and C) where S represents the sum of two single bit numbers and C represents the carry. It is the foundational arithmetic operation performed by VLSI systems. Mathematically ,S=A'B+AB' and C=AB. The inputs of half adder are called augends and added bits. There are 2 types of adder, half adder which takes 2 inputs and generate carry and sum , full adder which takes the previous carry also as input The simple half adder design has a XOR gate for sum and AND gate for carry. MUX is used as a data selector that selects one input and redirects to selected data with single output line. A multiplexer has 2^n inputs, n selection lines and only one output. A multiplexer which as two inputs and one selection line is known as 2 x 1 MUX . We require two 2 x 1 MUX for designing the half adder circuit ,the first digital inputs is used as input for the MUX and the other is used as selection line for the carry and sum block. The two inputs of the first MUX is the first digital input(A) and it's inverted input(A'). The two inputs of the second MUX is "Zero" and "A". The output of the first MUX is the Sum and the other is carry of the two Binary digits added. For A' input invertor is used and for "Zero" it is directly connected to ground or connected to 0V. Whenever the Input B is low the output of the second MUX results to zero.

2 Implemented Circuit

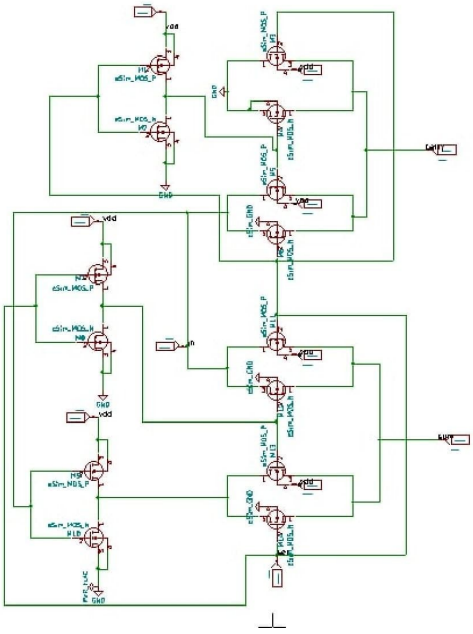

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

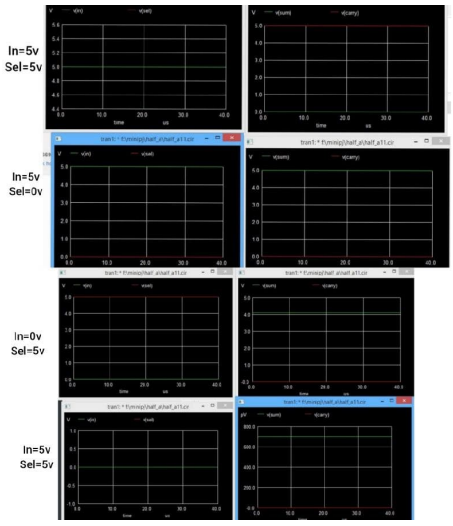

Figure 2: Implemented waveform.

References

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[2] D. K. R. Dayall. Multiplexer –based design of adders for low power vlsi applications. https://www.irjet.net/archives/V7/i6/IRJETV7I6493.pdf.