2:1 multiplexer using CMOS 130nm technology

SAYEEDURRAHMAN, ZHCET, Aligarh Muslim University

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Abstract

This paper presents an analysis on different parameters of 2:1 MUX using CMOS logic circuit with skywater130nm technology. Circuit is designed by using eSIM and then after converting Kicad to ngspice simulation is done by ngspice tool at 1.8V power supply. It is found that 2:1 MUX using CMOS consumes 99 percent less power than PTL(pass transistor logic). CMOS based 2:1 MUX utilizes 10 number of transistors. It is a combinational logic circuit used to select only one input among several inputs based on selection lines. Since multiplexer implemented by PTL utilizes minimum number of transistors is 2 but ouput is distorted. CMOS provides complete '1' and '0' logics at the output without any distortion.
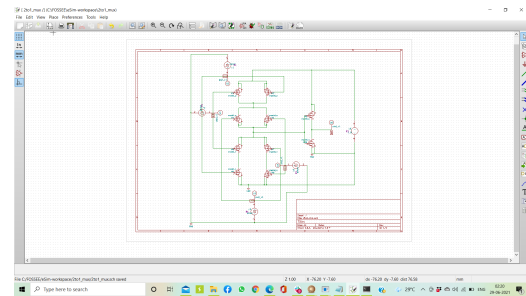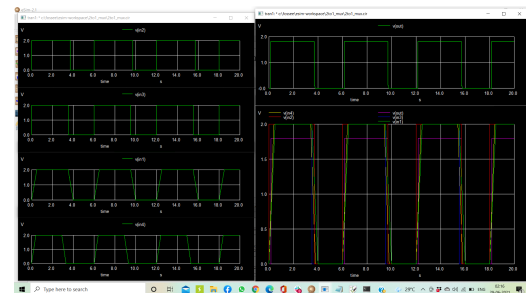
1 Circuit Details

In Complementary metal oxide semiconductor logic, it deploys symmetric number of both MOSFETS, i.e; PMOS and NMOS. Since, NMOS is strong '0' device and PMOS is strong '1' device. Hence, it leads to better performance of any logic circuit. CMOS provides complete '1' and '0' logics at the output without any distortion. 2 line to 1 line MUX using CMOS is simulated at sky130nm technology. As technology decreases, power consumption is also decreases. Logic circuit of 2 line to 1 line MUX consists of two AND, one OR and one NOT gate. Here the reference circuit attached is made up of using CMOS technology. In this circuit there are four PMOS and four NMOS used. The two PMOS are connected in parallel with series to two PMOS connected in parallel as shown in the reference circuit. And the two NMOS are connected in series with parallel to two NMOS connected in series When the input is low(0) NMOS is off and PMOS is on. Hence, the output is connected to Vdd through PMOS. When the input logic is high(1) PMOS is off and NMOS is on. Hence, the output is connected to ground through NMOS. And the overall output is inverted through inverter containing one PMOS and one NMOS. In order to efficiently use the Silicon, IC Manufacturers fabricate multiple Multiplexers in a single IC. Generally four 2 line to 1 line multiplexers are fabricated in a single IC.

2 Implemented Circuit

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

Figure 2: Implemented waveform.

References

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