# Low power NAND gate based full subtractor using CMOS Technology

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July 1, 2021

## Abstract

The modern electronic circuits are becoming more powerful and complex over a period of time because of the need for faster and efficient circuits. Portable devices like mobile phones which are powered by batteries should be designed in such a way that the power consumption is as low as possible to provide a long battery life. The CMOS technology paves way for designing circuits which are faster and efficient with better noise immunity than TTL circuits. The purpose of this paper is to provide an approach towards designing a full subtractor circuit using CMOS technology and to understand the functioning of the circuit by designing and simulating the circuit in eSim which is an open source EDA tool.

## 1 Circuit Details

The CMOS full subtractor can be implemented using 18 PMOS transistors and 18 NMOS transistors. To implement the full subtractor circuit the truth table of the full subtractor is constructed initially. The Karnaugh map is used to find the boolean expression for the difference and borrow outputs from the truth table. According to the boolean expression the CMOS full subtractor ciruit can be implemented using nine NAND gates. The nine NAND gates are implemented in CMOS Technology using complementary PMOS and NMOS enhancement mode mosfets. According to the boolean expression two XOR gates are required to generate the difference output. Each XOR gate is implemented using four NAND gates and the two XOR gates are cascaded to obtain the difference output. The two inputs of the remaining one NAND gate is connected to the intermediary stages of the two XOR gates in difference circuit according to the boolean expression to generate the borrow output. The inputs for the circuits are provided using pulse voltage sources with different time periods and time delays to simulate all possible combination of input for the circuit. The voltage probes are connected to the inputs and outputs of the circuit. The transient analysis is performed for a fixed amount of time and the voltages at the inputs and outputs of the full subtractor circuit are plotted on a graph.

## 2 Implemented Circuit

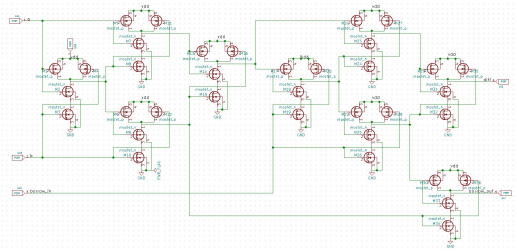

Figure 1: Implemented circuit diagram.

## 3 Implemented Waveforms

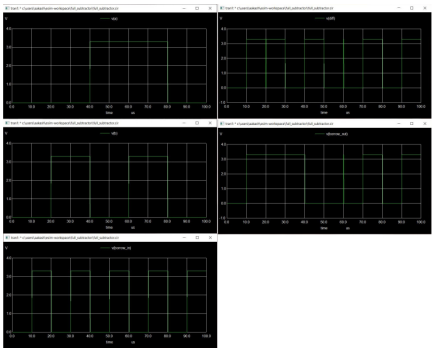

Figure 2: Implemented waveform.

## References

[1] R. L. M. J. B. D. S. J. R. G. S. K. J. T. D. Angelo A. Beltran, Kristina C. Nones. Low power nand gate based half and full adder subtractor using cmos technique. https://journal.umy.ac.id/index.php/jrc/article/view/8832.