Design of Exclusive-OR Gate using CMOS and SKY130 PDK technology

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Abstract

This reference paper recapitulates the design of the Exclusive-OR gate, also known as the XOR gate. This circuit is the basic block of combinational logical operations like AND, OR, and Inverter. This paper describes the function and operation of the XOR Gate. The output of XOR gives logic high when both the inputs are of opposite logic and gives logic low when both the inputs are of the same logic. This XOR gate is designed by Static CMOS design using eSim and SkyWater SKY130 PDK technology at the scale of 130nm and simulated successfully. The schematic diagram and its details with the Ngspice waveform are as follows.
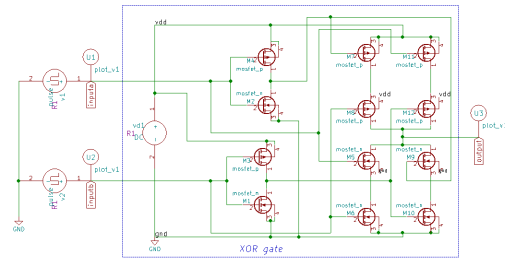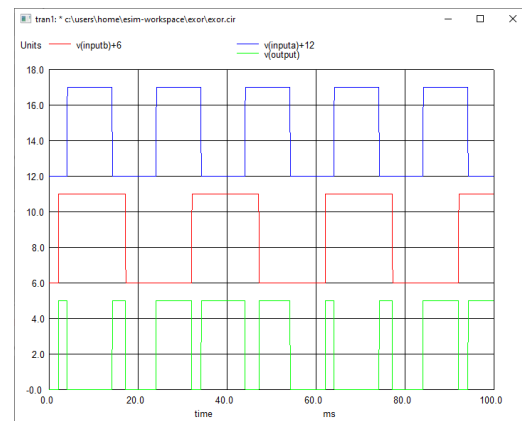
1 Circuit Details

The XOR circuit is the most fundamental unit of various Boolean and arithmetic circuits like adders, multipliers, parity checkers, and generators used for error detection. Static CMOS is the most widely used technology to design logic systems. The prime advantage of static CMOS design is low sensitivity to noise and consumes very low power through which gives a good performance. A static CMOS design is a combination of two networks pull-up network and pull-down network, pull-up networks provide the connection with Vdd and pull-down provides the connection with the ground. Two different combination rules are used in static complementary CMOS design. For NMOS, series combination implements AND operation, and parallel combination implements OR operation. For PMOS, series combination implements NOR operation, and parallel combination implement NAND operation. In the circuit shown, the schematic is divided into two parts the upper part constitutes the only PMOS and the lower part constitutes only NMOS. PMOS part is connected to Vdd and NMOS part is grounded to Vss. As we need original inputs and their complement too, so here I used two Inverters for each Input. There is a total of three plots used to plot the waveforms of Inputs and output with a global label that can be seen in my schematic diagram. I connected Vdd and Gnd to a DC source of 5v. For input, we used a pulse source. As the result, we got desired waveforms.

2 Implemented Circuit

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

Figure 2: Implemented waveform.

References

[1] T. L. Floyd. Digital fundamentals. https://g.co/kgs/5mQvLo.

[2] T. Sharma and L. Kumre. A comparative performance analysis of cmos xor xnor circuits. https://ieeexplore.ieee.org/document/8378202.