2-INPUT CMOS NAND GATE

Harish krishna R, PSG College of Technology

July 18, 2021

Abstract

Today, the most popular MOSFET technology is CMOS technology. This is the dominant semiconductor technology for microprocessors, microcontroller chips, memories like RAM, ROM, EEPROM and application-specific integrated circuits. NAND Gate is the combination of AND Gate and NOT Gate. It is one of the universal gates as it can be used to perform other logics like AND, OR and NOT. NAND logic finds its applications in Burglar alarm, freezer buzzer etc. This report presents a two input CMOS NAND gate designed using eSim. The MOSFETs used in this project are from Skywater SKY130 model library. SPICE simulations were performed using ngspice and desired output is obtained.

1 Circuit Details

CMOS technology provides two types of transistors. An n-type transistor and a p-type transistor. These are referred as nMOS and pMOS respectively.

A 2-input CMOS NAND gate consists of two series nMOS transistors between output and GND and two parallel pMOS transistors between output and VDD. If either of the two inputs is 0, at least one of the nMOS transistors will be OFF, breaking the path from output to GND. But at least one of the pMOS transistors will be ON, creating a path from output to VDD. Hence, the output will be 1. If both inputs are 1, both of the nMOS transistors will be ON and both of the pMOS transistors will be OFF. Hence, the output will be 0. Similarly, if both the inputs are 0, both of nMOS will be OFF and both of the pMOS transistors will be ON. Hence, the output will be 1.

The circuit diagram shown is designed using eSim. After electrical rues check the spice netlist is obtained. Then the eSim MOSFETS were replaced with sky130 MOSFETS. The pins are connected to appropriate ports. A constant DC voltage of 1.8 is given as Vdd. The vin1 and vin2 are pulse inputs. The output is obtained using vout port.

The pulsing characteristics of vin1 and vin2 are as follows. The initial values of vin1 and vin2 are 0 V. The pulsed value of vin1 and vin2 are 1.5 V and 1 V respectively. The pulse width of vin1 and vin2 are 5 microseconds and 10 microseconds respectively. The period of vin1 and vin2 are 10 microseconds.

The modified netlist with sky130 models was simulated using ngspice and desired waveforms were obtained.

2 Implemented Circuit

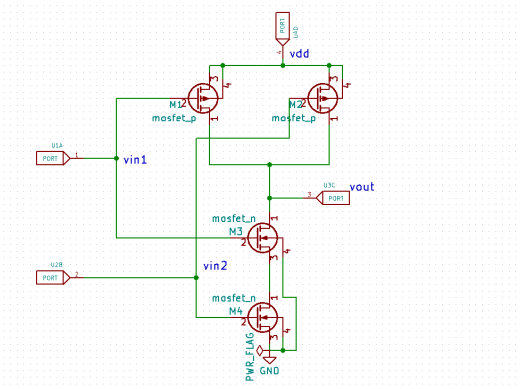

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

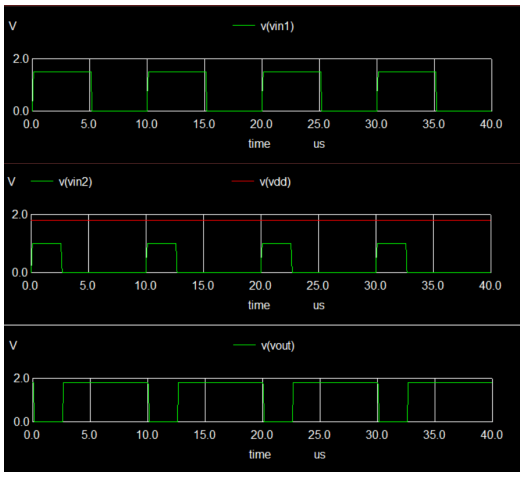

Figure 2: Implemented waveform.

References

[1] D. M. H. N. H. E. Weste. Cmos vlsi design a circuits and systems perspective. http://pages.hmc.edu/harris/cmosvlsi/4e/index.html.