NOR Gate - CMOS Technology.

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Abstract

NAND and NOR Gates are the two universal logic gates and any other logic gates can be built using them. A NOR gate i.e Negated OR gate is a logic gate with at least two and just one output with the opposite behavior of the OR gate. If all the inputs of this gate are false, then its output will be true. If at least one of the NOR gate's inputs are true,then the output of the gate will be false.Two input NOR gate using nmos and pmos is constructed. Various techniques at the different levels of the design process have been implemented to reduce the power dissipation, architectural and system level.

1 Circuit Details

The circuit consists of two pmos in series which forms Pull Up Network and two nMOS in parallel which forms Pull Down Network.Operation: When A=0 and B=0, both the nMOS transistors are OFF and both pMOS transistors are ON. Hence, the output is connected to VDD and we get logic high at the output. When A=1 and B=0, the upper pMOS is ON and lower pMOS is OFF, so the output cannot be connected to the VDD . Under this condition left nMOS is ON but right nMOS is OFF. Hence, the output is connected to ground we get logic low at the output. When A=0 and B=1, the upper pMOS is ON and lower pMOS is OFF, so the output cannot be connected to the VDD. Under this condition left nMOS is OFF but right nMOS is ON. Hence, the output is connected to ground we get logic low at the output. When A=1 and B=1, both the nMOS transistors are ON and both the pMOS transistors are OFF. Hence the output is connected to the VDD.The logic or Boolean expression given for a logic NOR gate is that for Logical Multiplication which it performs on the complements of the inputs. The Boolean expression for a logic NOR gate is denoted by a plus sign,with a line or Overline, over the expression to signify the NOT or logical negation of the NOR gate giving us the Boolean expression of: Y=(A+B)'.Logic NOR Gate is given a symbol whose shape is that of a standard OR gate with a circle, sometimes called an "inversion bubble" at its output to represent the NOT gate symbol with the logical operation of the NOR gate

2 Implemented Circuit

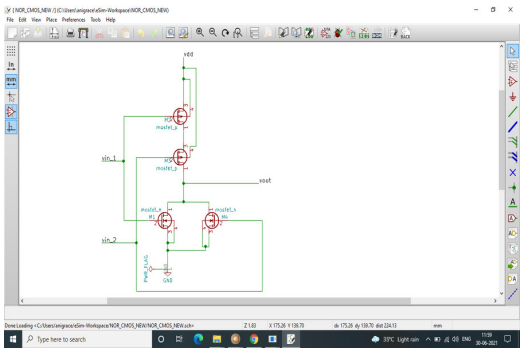

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

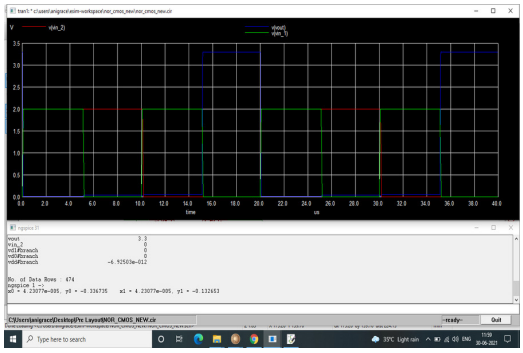

Figure 2: Implemented waveform.

References

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