D Flip Flop

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July 1, 2021

Abstract

D Flip Flop is a sequential circuit used highly in analog and digital systems to implement binary counters, shift registers etc. In this paper they have used cadence device at 90nm and 45nm technology. Delay flip flops stores whatever input pattern in its D input. So it is helpful to process the data bit by bit to get solutions for complex functions. It is known as Data flip flop since it can store data. Flip flop have each of two steady condition, logic 1 or logic 0. Triggering needs to be done to get any one of the two stable states.Delay flip flop is used to store the input bit pattern applied at its D input. The major drawback of the Set Reset flip flop is conquer through the D flip-flop.

1 Circuit Details
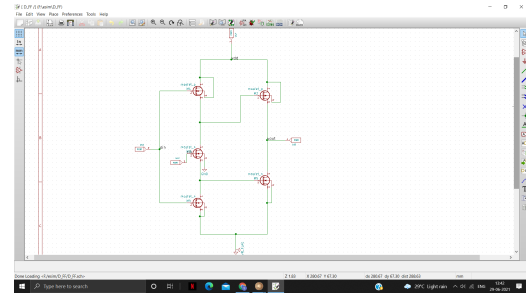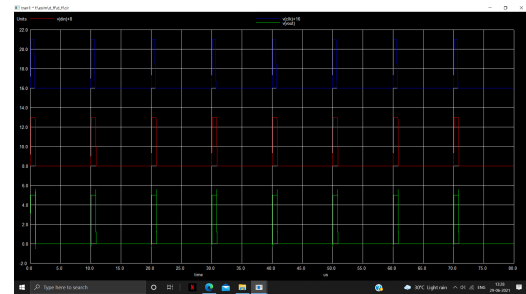
Flip Flop contains of 2 logics that is 0 and 1. Hence triggering needs to be done to get stable state out of these two. We can do such by applying an external pulse as input. The output remains in the same condition until the other pulse comes in. D Flip flop is designed by using 2 PMOS and 3 NMOS transistors. Clock is given to 1 of the NMOS and Digital input is given to NMOS and PMOS. There are 2 kind of flip flop solitary that is Single edge Triggered and Double edge Triggered. Now here TSPC D flip flop with 5 transistors is designed. TSPC stands for True Single Phase Clocked logic. TSPC performs exclusion of skews which reserved fragment region and power consumption. When Clk and Din are fed P1, N3 goes off and remaining P2, N1, N2 turns on. We know that the SR flip-flop requires two inputs, i.e., one to SET the output and another to RESET the output. By using an inverter, set and reset can be the outputs with only one input as now the two input signals complement each other. So by using the basic operations of nmos and pmos the d flip flop has been designed using sky 130 as well. In sky 130 I had to replace all the pmos and nmos with its instances. To plot also I have used sky 130 in a single graph. We can refer the truth table of D flip flop from any source and compare. The output what I was getting was similar to the output given in reference waveform.

2 Implemented Circuit

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

Figure 2: Implemented waveform.

References

[1] S. A. Madhu Shakya. Design low power cmos d flip flop using modified svl techniques. https:www.ijrar.org/papers/IJRAR1944229.pdf.