DESIGN OF 2-4 DECODER IN DIFFERENT CMOS LOGIC STYLES.

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Abstract

This brief presents a review on VLSI line decoders which are designed using various logic styles such as Complementary MOS (CMOS) Logic pass transistor pseudo-NMOS logic . A comparative study of the three mentioned logic families is represented based on their design style along with simulated propagation delay power and area (in terms of number of MOSFETs). CMOS Logic styles are more robust to low voltages designs have full-swing in output for specific input combinations pass transistor designs have fast restoring capability moderate speed and moderate power-dissipation and pseudo-NMOS logic provides high speed operation and require low transistor count.

1 Circuit Details

DECODER: A 2-4 line decoder has two inputs and four outputs. For Active High Output (AHO) decoders, for each possible input only one of the outputs is high and the others are low. This is vice versa for Active Low Output (ALO) decoders. AHO decoders are used in building multiplexer.

MOSFET is implemented as switch in all logic styles. If Logic '1' input is given to the gate of n-MOS, it acts as closed switch and its status would be considered as "ON" state. When the same logic '1' is applied to p-MOS it works as open switch which is assumed as "OFF" state. PASS TRANSISTOR: Pass transistor logic (PTL) was mainly developed in the 1990s when various design styles were introduced, aiming to provide a viable alternative to CMOS logic and improve speed power and area. Its main design difference is that inputs are applied to both the gates and the source/drain diffusion terminals of transistors. Pass transistor circuits are implemented with either individual nMOS/pMOS pass transistors or parallel pairs of nMOS and pMOS called transmission gates. PSEUDO-nMOS: The CMOS pull up network is replaced by a single pMOS transistor with its gate grounded. Since the pMOS is not driven by signals it is always 'on'. The effective gate voltage seen by the pMOS transistor is Vdd. Thus the overvoltage on the p channel gate is always Vdd minus VTp. When the nMOS is turned 'on' a direct path between supply and ground exists and static power will be drawn. However the dynamic power is reduced due to lower capacitive loading.

2 Implemented Circuit

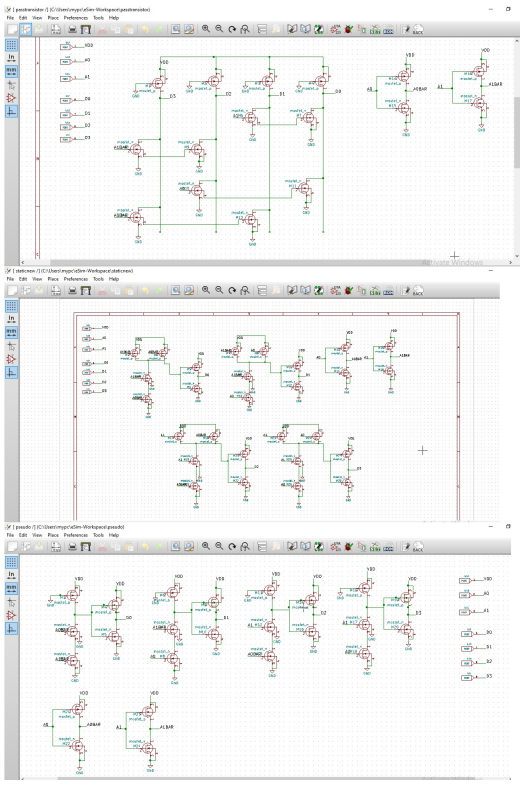

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

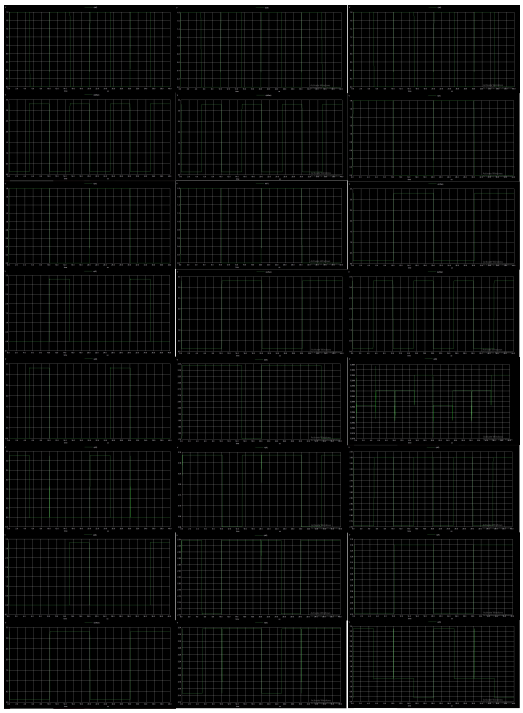

Figure 2: Implemented waveform.

References

[1] D. P. K. G. S. K. B. Srikanth, M. Sri Hari. " design and implementation of low-power, high-performance 2-4- and 4-16-line decoders using adiabatic logic circuits". International Journal of Engineering and Advanced Technology (IJEAT) ISSN: 2249 – 8958, Volume-9 Issue-1, October 2019.