4-Bit Parity Generator

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Abstract

This is the implementation of CMOS based four-bit Parity Generator. here we have used XOR-XNOR modules to design this circuit. The six transistors XOR-XNOR module involved in the design of parity generator is basic fundamental unit simultaneously giving XOR-XNOR output. Stacking Technique has been used to improve the conventional design. Power supply has been varied from 3.3 Volts for the proposed and basic design for 130nm PDK. The proposed circuit will be implemented in eSim EDA tool and will be done using Sky Water's 130nm PDK. eSim is the open tool for circuit design and Sky Water's 130nm Pdk was open source by google to designing chips.

1 Circuit Details

Parity generator plays an integral part in digital communication for correcting and detecting the error. Whenever we transmit the data from one point to another point then noise gets marred into the data which has been send. Due to this there is chance of message transformation in bit form which can change from 0 to 1 or 1 to 0. To done away all these miseries we add parity bit at the last of the message signal depending the no. of ones in that message if no. of ones are odd then to make odd parity we add 0 or vice versa and if no. of ones are odd then to make the even parity we add the 1 at the last of the message signal. Most of the electronic devices like communications devices have limitations in terms of power consumption. this can be reduced by using Stacking Technique. In this method every transistor is divided into two transistors each have W/L is half of the parent transistor. when the 4 inputs of the circuits contains odd number of 1s then the output will be 1, otherwise 0. the xor-xnor circuit was taken as block for simplification of circuit. First two bits was given to one block as input and next two to another. the xnor output of the two blocks was given to input as next block. so that xnor ouput of last block was even parity bit and xor ouput was the odd parity bit. This how the circuit designed.

2 Implemented Circuit

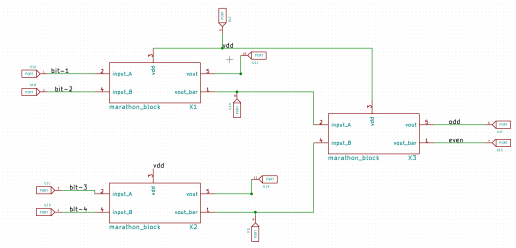

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

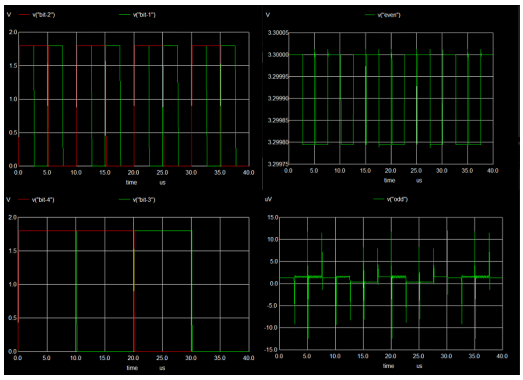

Figure 2: Implemented waveform.

References

[1] C. R. P. R. Bhargava Yasasvi. Implementation of parity checker using cmos logic techniques. https://ijari.org/assets/papers/6/2/IJARI-EE-18-06-103.pdf.

[2] S. W. A. Shukla. Design of odd-even parity generator using six transistors xor-xnor module. https://www.irjet.net/archives/V6/i11/IRJET-V6I1124.pdf.