DESIGNING AND IMPLEMENTATION OF SR FLIP-FLOP USING SKY130 Technology

Joji Jose, Government Engineering College, Idukki

July 1, 2021

Abstract

In a very large scale integration of integrated circuit (IC) nowadays, digital circuit with low power design is the target of the IC designer. In this paper designing and implementation done on low power and high speed SR flip flop using CMOS technology. Flip-flop is the primary place of memory elements to use on any portable device, a wide attention to reduce energy consumption flip-flop will help reducing energy consumption in a large IC. In this paper, we designed a flip-flop with CMOS logic; It consumes less energy than conventional gates designed. Switching transistors occurs when applied input clock is applied. The proposed SR flip flop is designed in esim and implemented using 130 nm in SkyWater Technology.

1 Circuit Details
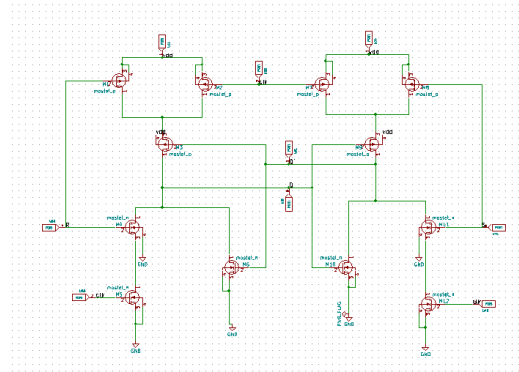
The relevant choice of flip-flop topologies is an essential step in the design of VLSI integrated circuits for high-speed and high-performance CMOS circuits. Understanding the suitability of flip-flops and selecting the best topology for a given application is an important criterion to fulfill the need of design to satisfy low power and high-performance circuit. The SR flip-flop is the most basic sequential logic circuit known as SR Latch. . The term "Flip-flop" relates to the actual operation of the device, as it can be "flipped" into one logic Set state or "flopped" back into the opposing logic Reset state. This act as the bistable device that has two inputs, one is "SET" meaning the output =1 and another is "RESET" meaning the output =0. Hence the SR circuit stands for "Set-Reset". Notice that when inputs S = "1" and R = "1" Q and Q' can be either logical levels "1" or "0" output, depending on state of S or R input, given input . Therefore, the condition of S = R = "1" does not change the status of output Q and Q'. However, the input state S = "0" and R = "0" is an undesirable condition or invalid and should be avoided. The condition S = R = "0" causes both output Q and Q' together to be high logic level "1" when reverse is usually Q. Q is losing the result of the check is that flip-flop Q and Q' , And where the two inputs are now switched "high" after logical condition "1". If S= 0;R=1 then Q = 0; Q' = 1 so flip flop is reset. If S = 1;R=0 Q = 1; Q' = 0 so flip flop is set.
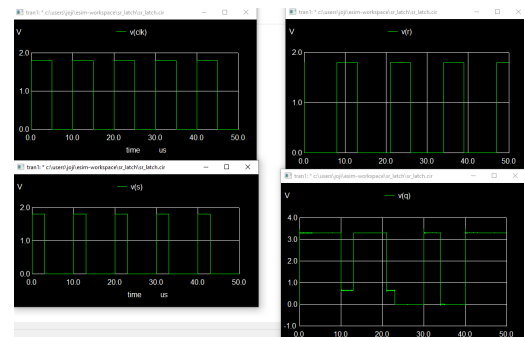
2 Implemented Circuit

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

Figure 2: Implemented waveform.

References

[1] T. point. Clocked sr latch. https://www.tutorialspoint.com/vlsi_design/vlsi_design_sequential_m