SRAM cell using TRIMODE MTCMOS power and ground gated technique

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Abstract

Static random access memory (SRAM) in which data is not written permanently and it does not need to be refreshed periodically. The main idea is to design a SRAM cell to reduce leakage power without affecting its performance. 10T SRAM architecture is proposed which operates in three modes, active, park, standby or hold. It provide better stability and reduced delay in active mode, reduced leakage current in standby mode and retaining the logic state in park mode. The cell consists of ten transistors in which four are high Vt transistors which are slow but have a low subthreshold leakage current and six are low Vt transistors are fast but have a high subthreshold leakage current

1 Circuit Details

The reference diagram of 10 T SRAM cell using TRIMODE MTCMOS power and ground gated circuit is shown in Figure1. The high Vt transistors are controlled externally by sl0, sl1, sl2 and sl3.In active mode the word line wl, sl2 and sl3 are made high, sl0 and sl1 are made low. This causes p2 and n5 transistors to be turned ON and p3 and n4 are turned OFF allowing virtual power line voltage to be equal to supply voltage and virtual ground line voltage to be at zero volts. In this case SRAM cell performs its operations efficiently. The power measured in this mode is dynamic power. In standby mode, the word line wl, sl1 and sl2 are made low, sl0 and sl3 are made high. This causes p2 and n5 and n4 and p3 to be turned OFF, cutting off power supply and ground terminal from SRAM cell thereby reducing the leakage power. The power measured in this mode is static power. In park mode, the word line wl, sl0 and sl1 are made high, sl2 and sl3 are made low. This causes p2 and n5 are turned OFF and n4 and p3 are turned ON, virtual power line will be at voltage Vdd-Vt and virtual ground line will be at voltage Vss+Vt, so it helps in retaining the previous data stored in active mode and avoids data retention problem. The inputs are bl and blbar and outputs are q and qbar. Active mode is implemented and waveform is attached in the figure 2 and in this mode this 10T SRAM will work more efficiently.

2 Implemented Circuit

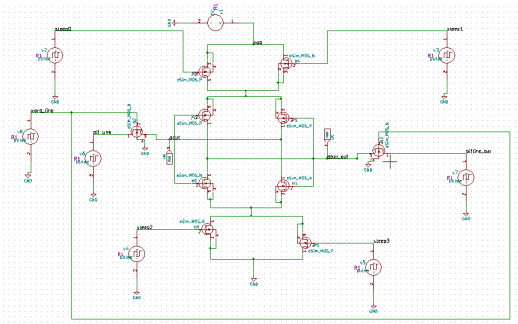

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

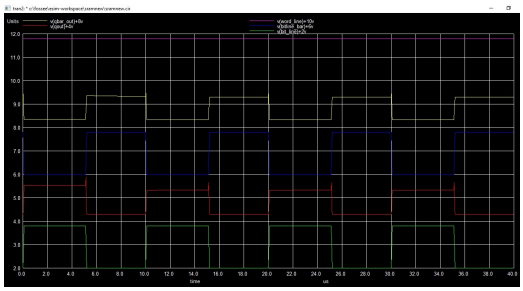

Figure 2: Implemented waveform.

References

[1] K. G. U. S. R. V. Malini. Design of novel sram cell using hybrid vlsi techniques for low leakage and high speed in embedded memories. https://link.springer.com/article/10.1007/s11277-019-06523-7.