

# CMOS NOR Gate

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## Abstract

There are various basic gates like inverter, NAND gate, NOR gate which are extensively used in the designing of the more complex circuits with higher number of transistors such as SRAM cells, MUXs, ADCs and various other circuits. Here, the NOR gate is studied. NOR gate is one of the basic logic gates to perform the digital operation on the input signals. A NOR gate, Negated OR gate, is a logic gate with at least two and just one output with the opposite behavior of the OR gate. NOR is a functionally complete operation, NOR gates can be combined to generate any other logical function. Hence, NOR gate is called Universal Logic Gate along with NAND gate.

## 1 Circuit Details

The logic circuit used to be called a NOT-OR gate because the output is  $Y$  equals  $\bar{A} + B$ , Read this as  $Y$  equals NOT  $A$  OR  $B$  or  $Y$  equals the complement of  $A$  OR  $B$ . Because the circuit is an OR gate followed by an inverter. NOR gates can be combined to generate any other logical function. It shares this property with the NAND gate. By contrast, the OR operator is monotonic as it can only change LOW to HIGH but not vice versa. In order to design 2-input NOR gate for equal rise and fall time, it is necessary to first design an inverter with equal rise and fall time. This involves compensating for the difference in electron and hole mobilities. For silicon material, the electron mobility is about 2.5 to 3 times greater than the hole mobility. Therefore, to have equal rise and fall time in an inverter, we must choose the  $W$  divide by  $L$  ratio of pMOS as 2.5 times greater than that of the nMOS transistor. A CMOS NOR gate circuit uses four MOSFETs its transistors are arranged in a two series connected sourcing transistors and two parallel connected sinking transistors. The transistors  $M1$  and  $M3$  work as a complementary pair, as do transistors  $M2$  and  $M4$ . Each pair is controlled by a single input signal. If either input1 or input2 are high at least one of the lower transistors will be saturated, thus making the output low. Only in the event of both inputs being low will both lower transistors be in cutoff mode and both upper transistors be saturated, the conditions necessary for the output to go high. This behavior of course defines the NOR logic function.

## 2 Implemented Circuit

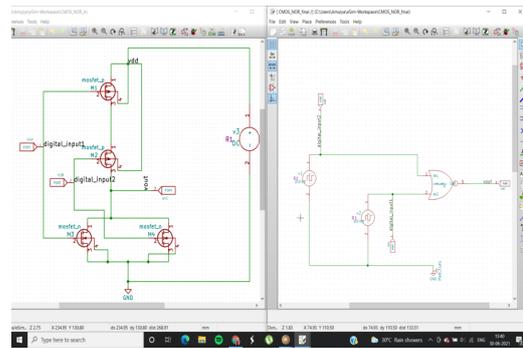


Figure 1: Implemented circuit diagram.

## 3 Implemented Waveforms

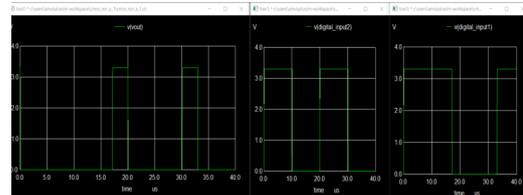


Figure 2: Implemented waveform.

## References

- [1] J. S. U. Balraj Singh, Mukesh Kumar. Analysis of cmos based nand and nor gates at 45 nm technology. [https://www.researchgate.net/publication/316548029\\_Analysis\\_of\\_C](https://www.researchgate.net/publication/316548029_Analysis_of_C)
- [2] T. R. Kuphaldt. Cmos gate circuitry. <https://www.allaboutcircuits.com/textbook/digital/chpt-3/cmos-gate-circuitry/>.