Transmission Gate Based Full Adder

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Abstract

By utilizing the transmission Gates , CMOS full adder created , which have less complex circuit than the conventional full adder . Computer recreations appear that they can realize the anticipated logical functions and they have alluring exchange characteristics . It'll take 3 inputs A in pulse , B in pulse and Cin in dc and allow 2 yields Carry in pulse and Sum in pulse . Its simulation will be done by E Sim, NG Spice and Sky130 Technology. it can be utilized in buildings block of on chip libraries , designed concurring to craved complexity of arithmetic and numeric computations

1 Circuit Details

By utilizing the transmission gates, the logic expressions of the CMOS full adders can be clarified palatably and their CMOS circuits can be for the most part disentangled. In CMOS technology, both N type and P type transistors are used to design logic functions. The same signal which turns ON a transistor of one type is used to turn OFF a transistor of the other type. A Transmission Gates is an electronic element and good non mechanical relay built with CMOS technology, It is made by Parallel Combination of NMOS and PMOS transistors. Full Adder is a arithmetic logic Circuit designed to add two single bit numbers with a carry, the full adder has Three input states and two output states i.e., sum and carry. In Transmission Gate based Full Adder, no need to supply Vdd, supply is provided by the Inputs itself. So, it reduces power. It has equal delay for Sum and Carry output.

Circuit Analysis 1.P is A XOR B, Bar P is AB + Bar AB Eq.1 Case 1 when A is 0. T1 is ON, P is B INV2 is ON, P is Bar B Case 2 when A is 1. T2 is ON, Bar P is B INV1 is ON, P is Bar B SUM S is A XOR B XOR Cin, which is P XOR Cin, Using Eq.1 Bar S is PCin + Bar PCin CARRY Co is PCin + AB, When P is 0, Co is AB When P is 1, Co is Cin If P is 0 then A=B, Bar Co is Bar A . So, Co is A.

Note Complement of A is Bar of A, Bar A. A,B are pulse but C is D.C.. So, the output will come according to it.

2 Implemented Circuit

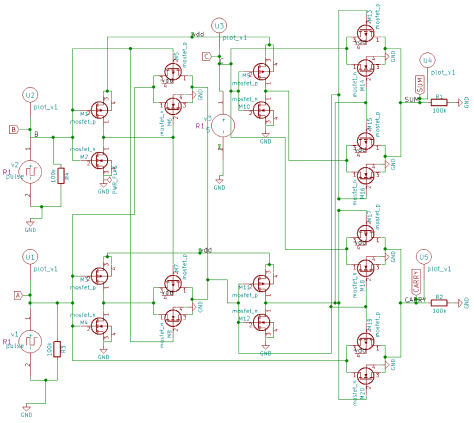

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

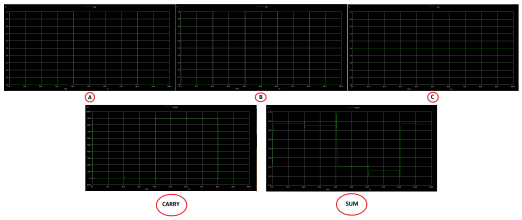

Figure 2: Implemented waveform.

References

[1] A. I. . . p. d. . Hindawi Publishing Corporation VLSI Design, Volume 2012. Performance analysis of high speed hybrid cmos full adder circuits for low voltage vlsi design. R. K. N. SubodhWairya and S. Tiwari.

[2] N. . M. . IEEE JOURNAL OF SOLID STATE CIRCUITS, VOL. 27. A new design of the cmos full adder. N. Zhuang and H. Wu.

[3] N. . F. . IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION VLSI SYSTEMS, VOL. 10. Performance analysis of low power 1 bit cmos full adder cells. I. T. K. D. S. M. I. Ahmed M. Shams, Member and I. Magdy A. Bayoumi, Fellow.