Design of CMOS Transmission Gate based 4:1 MUX using SKY130 PDK

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Abstract

This paper constitutes the design and analysis of 4:1 multiplexer (MUX) using CMOS transmission gate logic (TGL). A MUX is a combinational circuit, also known as data selector that combines multiple inputs into a single data stream. The basic logic behind the transmission gate used in digital CMOS circuit design is to pass or block a signal from the input to the output. It consists of parallel connection of both p-channel and n-channel MOSFETs. A MUX using transmission gate results in reduction of area compared to conventional CMOS based MUX. The circuit has been designed using SKY130 technology. "eSIM" open source EDA tool is used to design, simulation and analyze the circuit.

Keywords: TGL, MUX, SKY130, eSIM

1 Circuit Details

A Multiplexer is a device whose function is to select the input on any one of the multiple input lines and providing that input to the single output line. It is used to minimize the number of integrated circuitry required by a specific circuit design.

Transmission gate is the combination of back-to-back linked NMOS and PMOS where NMOS is placed in parallel with the PMOS device. NMOS device passes a strong 0 and a weak 1 whereas PMOS device passes a strong 1 and a weak 0. This arrangement acts as a switch that selectively blocks or passes a signal value from input line to output line. Thus an opposite signal is applied to the control gates such that both the transistors are either on or off. When the voltage on gate terminal of NMOS is Logic 1, then Logic 0 is applied to the gate terminal of PMOS, which allow both the transistors to conduct and pass the signal from the input node to the output node. When the voltage on gate terminal of NMOS is Logic 0, then Logic 1 is applied to gate terminal of PMOS, which turn off both the transistors and provide a high-impedance condition on both the input and output nodes. This design provides a bidirectional network without degradation of the input signal.

Architecture of a general 4:1 MUX comprised of 44 transistors whereas the transmission gate logic based 4:1 MUX consists of 12 transistors. Thus the power consumption is less with minimum area.

The circuit is simulated at nanosecond scale with 1.8V pulse voltage. The obtained output waveform verifies the truth table of 4:1 MUX.

2 Implemented Circuit

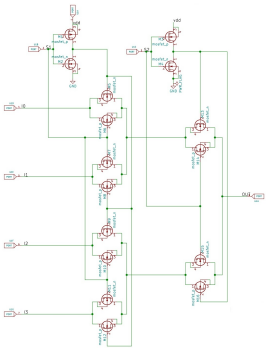

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

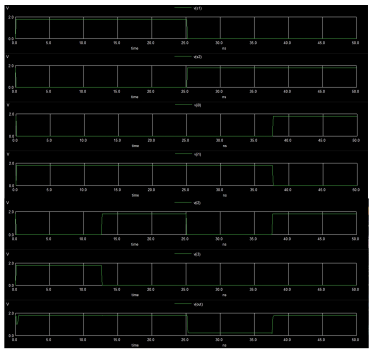

Figure 2: Implemented waveform.

References

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