2:1 MUX USING CMOS LOGIC

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Abstract

This study assesses a 2:1 multiplexer based on CMOS logic.Since a multiplexer is an important component of a communication system,an efficient design of MUX is required to increase the efficiency of data transmission,effectively utilise the vast memory space of a computer,and convert parallel form of data into serial form in telecommunication networks. The implementation is done in VLSI technology as it has features like small size, low cost, high operating speed and low power. The performance analysis of the MUX using CMOS logic families are conducted using eSim , ngspice and sky130 technology.
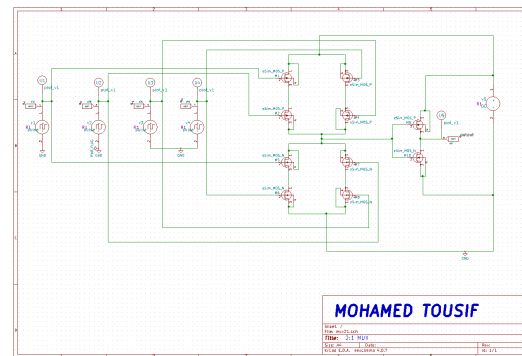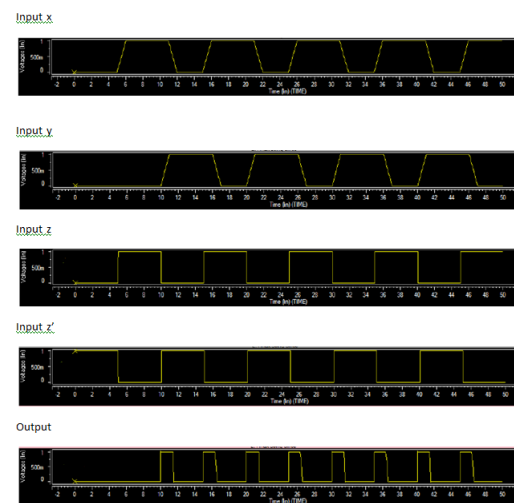
1 Circuit Details

Complementary Metal Oxide Semiconductor (CMOS) logic deploys symmetric number of both types of MOS-FETs, i.e., PMOS and NMOS. This leads to better performance of any logic circuit since NMOS is strong '0' device and PMOS is strong '1'device. Thus, CMOS provides complete '1' and complete '0' logics at the output without any distortion. A multiplexer is a combinational circuit that selects binary information from one of the many input lines and directs it to a single output line. As a result, in addition to the input and output lines, selection lines are utilised to pick a certain input line. The multiplexer is basically a data selector that chooses one of numerous digital or analog input signals and sends it to a single output line.A two-input multiplexer has n select lines that are used to choose which input line to send to the output. 2:1 MUX has 2 input data lines, single select line and single output line as well. When the binary value of select line is logic '0' then input 'x' is passed to the output line. When the binary value of select line is logic '1', then data line 'y' is connected to output line and transmitted through it. The Boolean expression of 2:1 MUX is as follows : Y=XZ'+YZ. 2:1 MUX using CMOS modelled using 10 transistors , input pluse generator and dc source and plot is used at the input and output to generate waveforms as shown in the diagram.

2 Implemented Circuit

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

Figure 2: Implemented waveform.

References

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