CMOS NAND GATE USING 130NM TECHNOLOGY

Ilka Shawl, Government College of Engineering and Technology, Ganderbal, Kashmir

June 29, 2021

Abstract

The digital logic NAND gate is a basic digital circuit used to operate on digital inputs. This easy to construct gate is a multiple input single output logic circuit which results in the complementary Boolean addition of all its inputs. It is a universal gate i.e. all the other logic gates can be designed using NAND gate. The output of the NAND gate is high (1.8V), only if all the inputs are low (0V), otherwise its output is low. The fabrication of NAND gate using CMOS or complementary MOSFET employs two pairs of pMOS and nMOS devices. The 130nm technology here refers to the fabrication of MOSFETs using Sky130 process.

1 Circuit Details

The schematic circuit diagram of the two input CMOS NAND gate demonstrates the employment of two nMOS and two pMOS transistor devices fabricated using 130nm technology. The nMOS transistor devices M3 and M4 are connected in series while the source terminal of M3 is grounded or at '0V'. Meanwhile, the pMOS transistor devices M0 and M1 are connected in parallel while the source terminals of both the devices are connected to a positive high voltage or Vdd or '1.8V'. The output is drawn from the drain terminal of all the four MOSFETs. When any of the logic inputs A or B or both are connected to logic low or '0V', the corresponding nMOS transistor device is driven into cut off mode due to the lack of gate to source potential and can be approximated to an open circuit while the corresponding pMOS gets into conduction mode as the negative gate to source potential is present and can be approximated to a short circuit. This results in the output voltage being Vdd or logic high or logic 1. When both the inputs are at logic high or '1.8V', both the nMOS transistor devices are short circuited owing to the presence of positive potential difference between their gate to source terminals while the pMOS is driven into cut off mode equivalent to the open circuit, producing the final output as 0V or logic low or logic 0. The final simulated implemented waveform confirms the operation of the circuit as a logic NAND gate.

2 Implemented Circuit

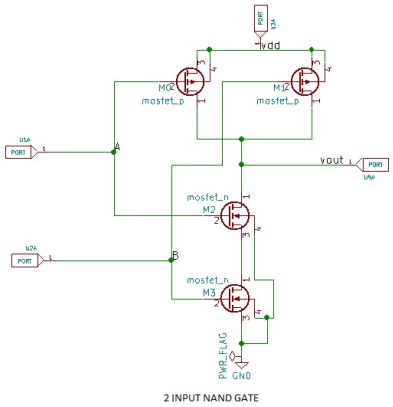

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

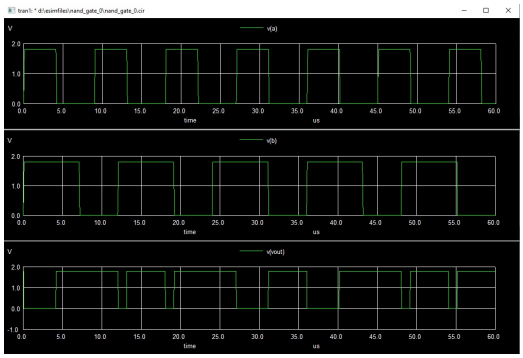

Figure 2: Implemented waveform.

References

[1] J. A. Núñez-Corona. Design of the analog transmitter module in 130 nm cmos technology. https://core.ac.uk/download/pdf/47250549.pdf.