TWO INPUT XOR GATE USING CMOS 130nm

FATIMA SHABIR ZEHGEER, government college of engineering and technology ganderbal kashmir

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Abstract

The two input XOR logic gate gives the high output when only one input is high and the other is low. This gate is an essential element in circuits like full adders, parity generators, checkers, etc. In this circuit, the XOR gate implemented using six MOS transistors instead of eight or so as in conventional CMOS XOR circuit. The circuit design is based on the pass transistor logic which has reduced the transistor count and offered low power operation with low propagation delay and thus high performance. Also due to the presence of feedback path, this circuit does not suffer signal deterioration.
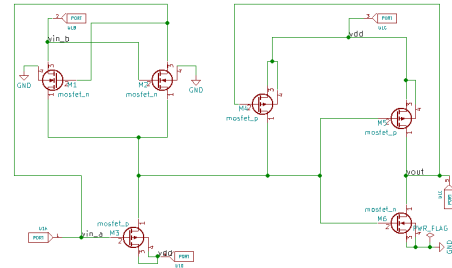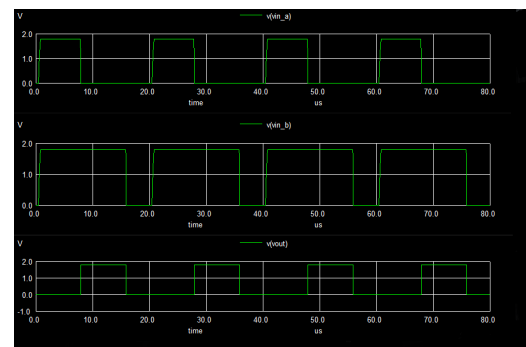
1 Circuit Details

Circuit uses 6 MOS transistors with M5 and M6 implemented as CMOS inverter. VDD, which is strongest source of 1 is connected to M3, M4 and M5.When A and B both will be 0 only PMOS transistor M3 will be ON. So, there will be direct path between VDD and input of CMOS inverter. Since PMOS is perfect switch in passing 1, strong 1 is passed to inverter. In inverter, NMOS M6 will be ON which provides discharge path from output to ground and thus the output will be 0.This output is applied through feedback path to PMOS M4 which is turned ON and passes strong 1 to CMOS inverter, generating 0 at the output. When A is 0 and B is 1 M3 and M2 will be turned ON which will pass 1 and 0 respectively. But for exclusive 0R implementation 1 is required at output and thus 0 is to be at the inverter input .For this width to channel length ratio of M2 is increased than that of M3. Hence 0 is passed to inverter input only and the output is strong 1. When A is 1 and B 0 only M1 is ON which passes a strong 0 to inverter and so output is logic 1.When both inputs are 1, M1 and M2 will be ON but NMOS is imperfect in passing 1, a degraded 1 is passed to inverter and output will be 0 but degraded. But due to feedback path M4 turns ON and passes perfect 1 to inverter resulting in perfect 0 at the output. Thus, two input exclusive OR gate is realized for all input combinations.

2 Implemented Circuit

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

Figure 2: Implemented waveform.

References

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