CMOS AS AN INVERTER CIRCUIT

Sudeshna Pahari, INSTITUTE OF RADIOPHYSICS AND ELECTRONICS, UNIVERSITY OF CALCUTTA

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Abstract

CMOS is also sometimes referred to as complementary symmetry metal oxide semiconductor. The words complementary symmetry refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p type and n type metal oxide semiconductor field effect transistors or MOSFETs for logic functions. CMOS inverters are some of the most widely used and adaptable MOSFET inverters used in chip design. They operate with very little power loss and at relatively high speed. Further more, the CMOS inverter has good logic buffer characteristics, in that, its noise margins in both low and high states are large.

1 Circuit Details

A CMOS, is basically an inverter logic or NOT gate, that consists of a PMOS at the top, and NMOS at the bottom, whose gate and drain terminal are tied together. The gate terminals of both the MOS transistors is the input side of an inverter, whereas, the drain terminals form the output side. The source terminal of PMOS is connected to Vdd, whereas source of NMOS is connected to Vss. There is a fourth terminal for a MOS transistor commonly referred to as Substrate terminal. It is connected to Vdd for PMOS and to Vss for NMOS. This is one of the terminals of MOS transistor, which could to be used to vary the threshold voltage of transistor by applying certain voltage to it. The propagation delay of an inverter is the difference in time or calculated at 50 percent of input output transition, when output switches, after application of input. Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Significant power is only drawn while the transistors in the CMOS device are switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor transistor logic or TTL or NMOS logic, which uses all n channel devices without p channel devices. Considering the static condition first, in region 1 for which Vin equals with logic 0, the p transistor fully turned on while the n transistor is fully turned off. Thus no current flows through the inverter and the output is directly connected to Vdd through the p transistor.
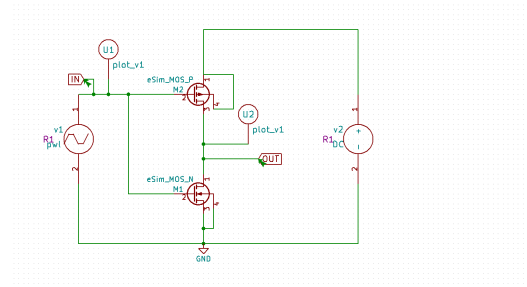
2 Implemented Circuit

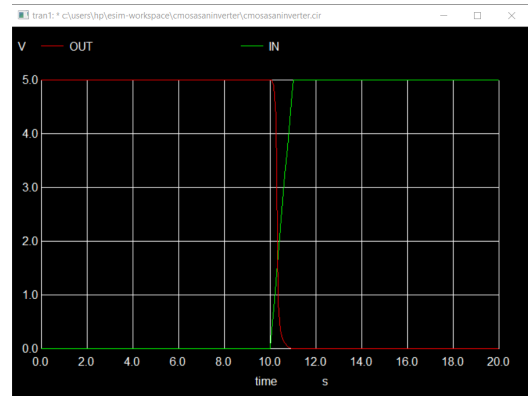Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

Figure 2: Implemented waveform.

References

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[2] S. V. L. I. I. O. T. GUWAHATI. Cmos inverter. https://vlsi-iitg.vlabs.ac.in/CMOS_theory.html.