2:1 MULTIPLEXER USING PASS TRANSISTOR LOGIC

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July 3, 2021

Abstract

Since multiplexer (MUX) is one of the important components of communication system, to increase the efficiency of data transmission.A multiplexer can be designed using various logic,like Static CMOS, Pseudo NMOS logic,Domino logic,Transmission Gate logic and Pass transistor logic etc. But our main motive is to design a 2:1 MUX using minimum no. of transistor. So here we can design a 2:1 MUX using Pass Transistor logic having only 4 MOSFETS(Including 2 MOSFETS for INVERTER).Using Pass Transistor logic to implement 2:1 MUX has an additional advantage of lower capacitance.Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages.

1 Circuit Details

This 2:1 MUX using Pass Transistor Logic consists of total 4 MOSFETS(Including 2 MOSFETS for INVERTER). First 'digital input' is inverted then inverted 'digital input' is connected to the gate terminal of M3 and 'digital input' is directly connected to the gate terminal of M4. We know from CMOS logic families, when Gate terminal's logic is '1' for a NMOS,then the NMOS acts as a short circuit and if logic '0', then it acts as a open circuit, and vice versa for PMOS. So, when Gate terminal logic is '1'of a NMOS,it allows to pass the input value. When Gate terminal logic is '0' of a PMOS,it allows to pass the input value. But here we only need 2 NMOS to implement 2:1 MUX(only 1 PMOS for INVERTER), Gate terminal of M3 is connected to inverted value of 'digital_input', so M3 will pass the input value of vin1 when digital input=0, similarly Gate terminal of M4 is connected directly to 'digital_input', so M4 will pass the input value of vin2 when digital input=1. Here, vdd=5v, digital input= a pulse input having 5volt as logic 1a nd gnd as logic 0, vin 1 and vin 2=a random digital sequence with 3 volt as logic 1 and 0v as logic 0. i choose, vin 1 as-010011 and vin 2 as-110101. as well as we can consider vin 1 and vin 2 as constant dc source so. In M1,sorce and body terminal is connected to gnd but in M3 and M4 sources are connected to vin 1 and vin 2 and body are connected to gnd.

2 Implemented Circuit

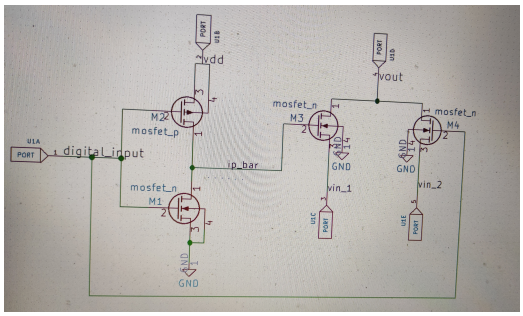

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

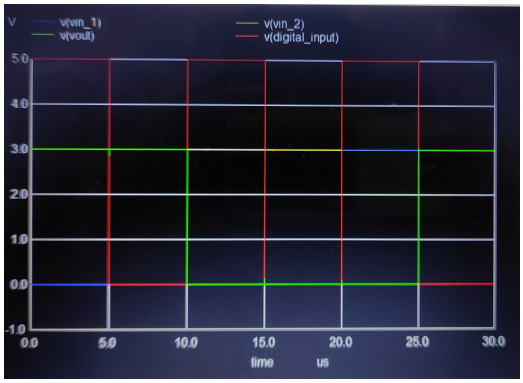

Figure 2: Implemented waveform.

References

[1] A. R. T. DUA. 2:1 multiplexer using different design styles: Comparative analysis. https://www.researchgate.net/publication/349211497_21_Multiplexer