Design and Analysis of Half Adder

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Abstract

This proposed abstract constitutes of the designing and analysis of half adder. It not only performs addition but can also be used to perform subtraction, division and multiplication. Hence, it can be considered as the key component in the designing of digital systems. Half adder is a basic building block in digital system and used to design full adder, carry look ahead adder and many more circuits. To perform addition on binary bits the Arithmetic and Logic unit present in the computer prefers this adder circuit. The half adder circuit is implemented using CMOS (Complementary Metal Oxide Semiconductor) which is considered to have more power and speed.

1 Circuit Details

The half adder implementation using CMOS consists of NMOS and PMOS. It consists of two inputs and two outputs which is sum and carry. If the two inputs are X and Y then, the sum will be XOR of inputs X and Y (X XOR Y) and the carry will be AND of X and Y (X AND Y). The sum and carry both will be low if both inputs X and Y are low. If X is high and Y is low or X is low and Y is high, the sum output will be high and carry will be low. For the case where both X and Y are high, there will be a carry generated (carry=high) and sum will be low. Logic circuits can be implemented using transmission gates. The circuits can be made compact using transmission gates which is a important consideration in silicon implementations. The transmission gate can conduct in both directions. Since the transmission gates conduct current in both the directions, the substrate terminals are connected to supply voltage inn order to make sure that the substrate diode is always operated in the reverse direction. The XOR gate is implemented using six transistors which is combination of NMOS and PMOS. The output of XOR will be set to high if the inputs are high and low or low and high. If the inputs are in same state that is, low and low or high and high then XOR will result in low state. The main advantage of using transmission gate design is that it passes both 0s and 1s effectively as follows. When NMOS is off and PMOS is on and it will pass logic Zero and logic one will be passed when PMOS is off and NMOS is on.

2 Implemented Circuit

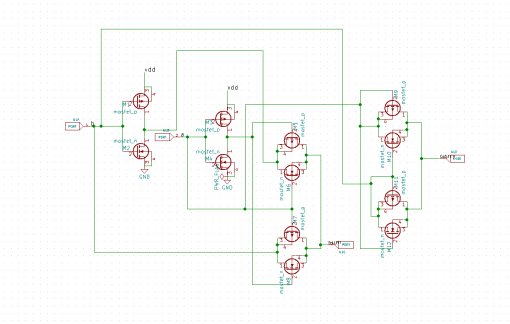

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

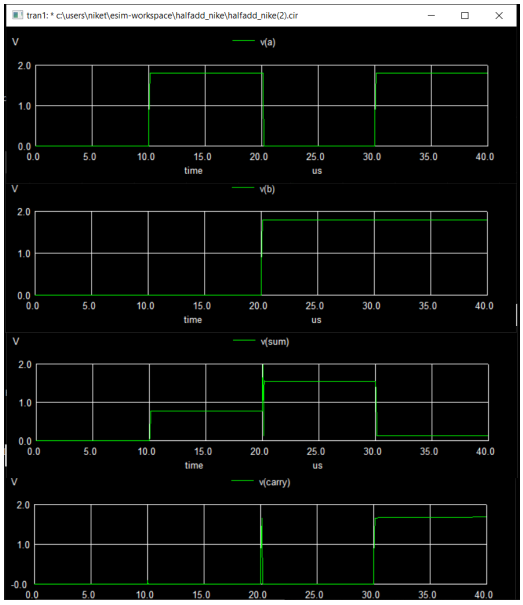

Figure 2: Implemented waveform.

References

[1] K. A. S. G. R. H. G.Naveen Balaji, V.Aathira. Combinational circuits using transmission gate logic for power optimization. https://www.researchgate.net/publication/304353741.