CMOS NOR Gate using SKYwater 130nm technology

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Abstract

In this paper, a two input CMOS NOR Gate is designed and simulated using eSim and SKYwater 130nm technology. A NOR Gate is a combination of OR Gate followed by a NOT Gate. It is the opposite operation of OR Gate where the logic NOR gate is complementary of OR Gate. The logic output of NOR Gate is HIGH (logic 1) only when the inputs are low (logic 0). NOR gates can be combined to implement any other logical functions and that is why they are also called as an universal logic gate. The CMOS NOR gate circuit consists of four MOSFETs , two PMOS in series connected to Vdd and two NMOS in parallel connected to gnd.

1 Circuit Details

The circuit shows the realization of a 2 input NOR Gate which consists of two PMOS transistors connected in series with each other forming the pull-up network and two NMOS transistors which are connected in parallel to each other forming the pull-down network. The NMOS transistors which are connected in parallel pulls the output low (logic 0) when any of the inputs to the circuit is high (logic 1). The PMOS transistors which are connected in series pulls the output high (logic 1) when both inputs to the circuit are low (logic 0). Here in this circuit , When both the inputs are low (logic 0), NMOS transistors will be open circuited (OFF) and PMOS transistors will be short circuited (ON) giving a HIGH (logic 1) at the output. When input Va is HIGH (logic 1) and input Vb is LOW (logic 0) , PMOS2 and NMOS1 transistors will be short circuited (ON) , PMOS1 and NMOS2 transistors will be open circuited (OFF) giving a LOW (logic 0) at the output. . When input Va is LOW (logic 0) and the input Vb is HIGH (logic 1) , PMOS1 and NMOS2 transistors will be short circuited (ON) , PMOS2 and NMOS1 transistors will be open circuited (OFF) giving a LOW (logic 0) at the output. When both the inputs are HIGH (logic 1) , the NMOS transistors will be short circuited (ON) and the PMOS transistors will be open circuited (OFF) giving a LOW (logic 0) at the output.

2 Implemented Circuit

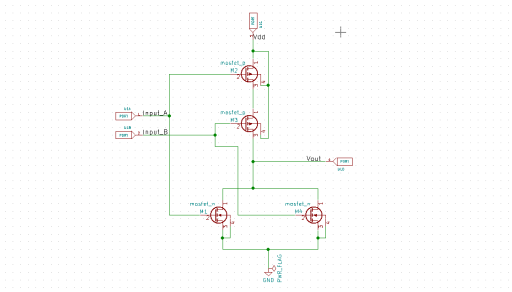

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

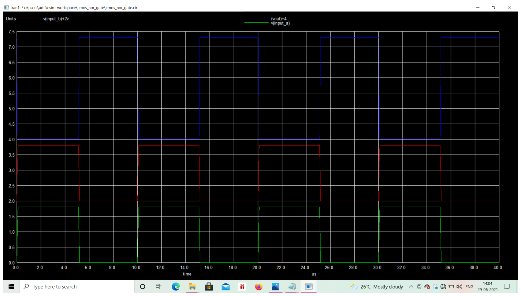

Figure 2: Implemented waveform.

References

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