

Low Noise Low Power Amplifier for Biomedical Applications

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Abstract

Implementation of EEG signal amplification using low power two stage amplifier. A Bulk Driven Folded Cascode structure is used. The presented amplifier delivers enhanced performance over that of the conventional folded. To reduce the flicker noise PMOS input transistors with large gate area are used. The presented amplifier is simulated in sky130 technology. Biomedical signals have weak amplitude and low frequency so we need to amplify these signals. Amplifiers should have basic features like high CMRR low power consumption low input referred noise for good performance in the field of biomedical engineering.

2 Implemented Circuit

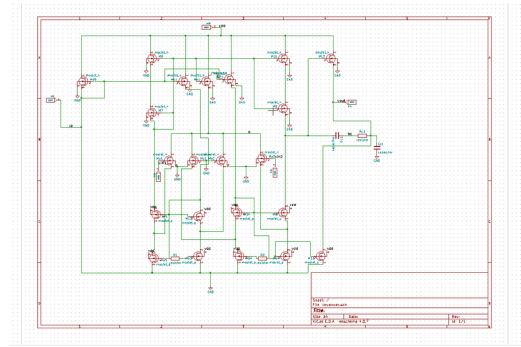


Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

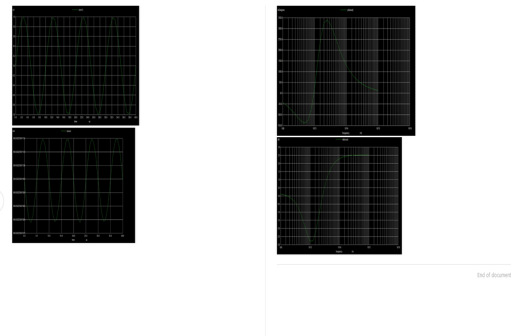


Figure 2: Implemented waveform.

1 Circuit Details

CMOS technologies paved way to increasing market of mobile and portable electronic devices. This growth is driven by the continual integration of complex analog and digital building blocks on a single chip. The operational transconductance amplifier is an important analog building block and for many applications is the largest and most power consuming. Recently, one of the most commonly used architectures whether as a single-stage or first stage in multistage amplifiers had been the folded cascode amplifier for its high gain and reasonably large signal swing in the present and future low voltage CMOS processes. Biomedical signals have weak amplitude and low frequency so we need to amplify these signals. Amplifiers should have basic features like high CMRR low power consumption low input referred noise for good performance in the field of biomedical engineering.

There are many ways to design the amplifier with above conditions. For example implementation here is two stage gate driven folded cascode amplifier. In addition to reduce the flicker noise PMOS input transistors with large gate areas are used for low power operation. I_b current in M_0 M_{c1} and M_{c3} is mirrored by M_b then M_0 supplies the first stage current. M_{13} and M_{14} currents are controlled by M_{c1} and M_{c2} . Equal drain potentials is maintained by M_{13} and M_{14} across the M_{a3} M_{b3} and M_{a4} M_{b4} in order to improve matching. C_c and R_c are used between the drain of M_8 and output terminal for compensation, So it improves the phase margin and GBW.

References

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