NAND Gate Design

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Abstract

There are various basic gates like inverter, NAND gate, NOR gate which are extensively used in the designing of the more complex circuits with higher number of transistors such as SRAM cells, MUXs, ADCs and various other circuits. In this paper, we have carried out the modeling of NAND gate and NOR gate at 45 nm technology. The modeling includes schematics design, layout design and layout vs schematic (LVS) run of the above gates. Also the simulation results of both the gates are obtained at the same node with rise time, fall time, area, delay and power dissipation (dynamic power and static power).

1 Circuit Details

The technological advancements leading to the shrinking of VLSI technology has to follow the various perspectives such as a decrease in the power dissipation, higher signal to noise margin (SNM), lower area, higher speed and lower cost etc [1]. As the technology is scaled down from higher node to lower node, these various aspects change accordingly. So depending upon the application and fabrication availability we use a particular node. Static CMOS are very power efficient as they dissipate nearly zero power while in idle state. These are frequently used for modeling of various designs. Taking into consideration of the history of CMOS design, power was secondary consideration after speed and area for many chips [2], [3]. But as the transistor counts and frequencies have increased, power consumption has shoot up rapidly and hence now is a primary design constraint [3]. Sub-threshold leakage power is already a major problem for battery powered designs in 45 nm node and will increase exponentially as power supplies and threshold voltages are scaled down further. Most of the power systems need higher performance when in active state and lower leakage when in μ idle state. This paper is organized into four sections. Section I provides general introduction about the low power designing and scaling effects.
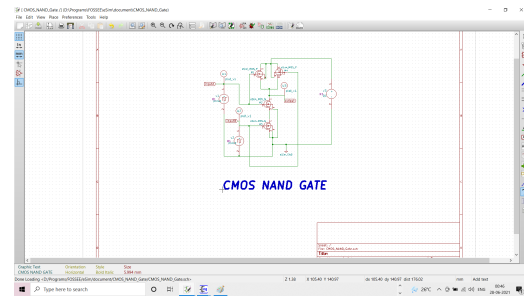
2 Implemented Circuit

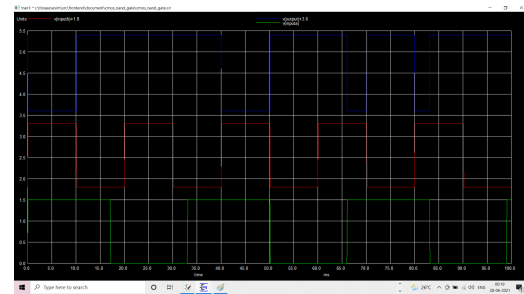Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

Figure 2: Implemented waveform.

References

[1] J. S. U. Balraj Singh, Mukesh Kumar. Analysis of cmos based nand and nor gates at 45 nm technology. https://www.researchgate.net/publication/316548029.

[2] I. Q. D. M. I. David Wolpert, Student Member and I. Paul Ampadu, Member. Nand gate design for ballistic deflection transistors. https://www.researchgate.net/publication/224610853.