8 bit Successive-approximation-register Analog-to-Digital Converter

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Abstract

Analog to Digital Converters (ADC) convert analog electrical signals to digital signals for data processing purposes. ADC's are widely used in data measurement, such as measuring analog voltages or currents and converts it to a digital number representing it's magnitude. There are many ADC architectures, namely Flash, successive approximation, pipelined, sigma-delta etc. Successive-approximation-register (SAR) analog-to-digital converters (ADCs) are frequently the architecture of choice for medium-to-high-resolution applications. Now a days, CMOS technology has become the most predominant for integrated circuit manufacturing. This technology is a very efficient in terms of power consumption.

1 Circuit Details

Main building blocks of a SAR-ADC are: sample &hold circuit, comparator, timing and logic control whichis mainly SAR logic, DAC (Digital to Analog Converter)in the feedback loop of ADC. The sample and hold circuit holds the input signal. The sample and hold circuit consists of a CMOS opamp configured as a buffer, followed by a CMOS switch. A capacitor holds the sampled signal while the conversion takes place. The SAR logic circuit consists of 8 bit register, where MSB is initially set to 1. This is converted to analog and compared with the input signal. If the input signal is greater than the DAC output, then comparator, again implemented using CMOS op amp, goes high. This keeps the MSB as 1. Else, if the DAC output is greater than input signal, comparator goes low and sets the MSB as 0. This is repeated for all the bits. The SAR logic is implemented using D flip flops. The D flip flops has been implemented using CMOS. A R-2R digital to analog converter (DAC) is used to convert the digital output back to analog for comparison in the comparator. This process is repeated until the conversion matches the digital equivalent. A basic component considered can be the CMOS opamp. The differential pair are implemented using both nmos and pmos. In this design, the nmos are the driving devices with pmos acting as a load to the nmos. The CMOS opamp considered, has a differential pair with single ended output.

2 Implemented Circuit

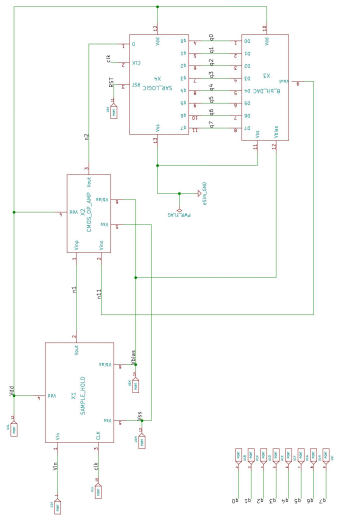

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

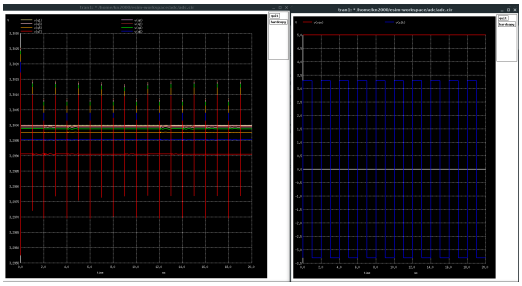

Figure 2: Implemented waveform.

References

[1] M. Integrated. Understanding sar adcs: Their architecture and comparison with other adcs. https://www.maximintegrated.com/en/design/technical-documents/tutorials/1/1080.html.

[2] B. Mazhari. Introduction to cmos analog circuits. https://home.iitk.ac.in/ baquer/EE610_CMOS_Analog_circuits.htm.