Design and Analysis of Two Stage CMOS Operational Amplifier

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July 16, 2021

Abstract

In this project, a two-stage CMOS operational amplifier is designed using the SkyWater 130nm PDK. The proposed two-stage op-amp consists of NMOS current mirror as a bias circuit, a differential amplifier as the first stage, and a common source amplifier as the second stage. The first stage of an op-amp contributed high gain while the second stage contributes a moderate gain. The results show that the circuit can work at 1.8V power supply voltage, provides a gain of greater than 60 dB, and the phase margin of the op-amp is nearly 60 degrees for a load of 2pF capacitor. Therefore, the power dissipation and the consistency of this operational amplifier are better than the previously reported operational amplifier.

1 Circuit Details

A low power operational amplifier is widely used as a bio-potential amplifier where it is used to amplify and filter extremely weak bio-potential signals. The first block is an input differential amplifier and it was designed to provide very high input impedance, low noise and also high gain. The output is single ended so that the rest of the op-amp did not contain symmetrical differential stage and since the transistors is operating in the saturation region, there is an appropriate dc voltage difference between input and the output signals of the input stage. Second block will perform level shifting, added gain and single to ended conversion. Level shifting is needed to compensate for dc voltage change occurring in the input stage so that an appropriate dc bias can be assured for the following stages. The added gain is used to provide gain or an additional amplification to the input stage as it is not sufficient. The conversion to single ended signal is performed in a subsequent stage as in some circuits, the input stage has a differential output. Proposed design specification are: Gain greater than 60dB; GBW equal to 30MHz; Phase Margin greater than 60 degrees; VDD equal to 1.8V; Load capacitance equal to 2pF; Length of the transistor equal to 500nm. Our main region of interest is Gain and Phase Margin in our analysis. Our simulation results show us that Gain is somewhere between 90 to 95 dB and phase margin is nearly equal to 60 degrees. This shows that our designed circuit is strictly following all our proposed design specification.

2 Implemented Circuit

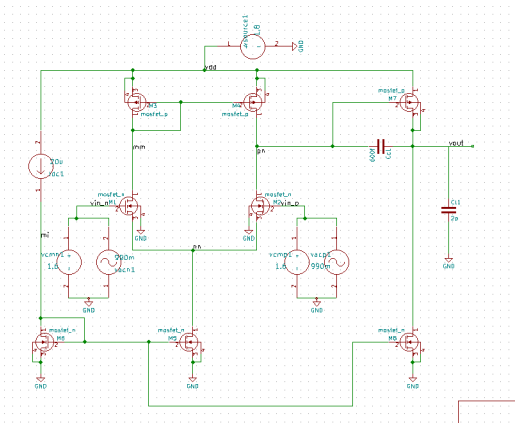

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

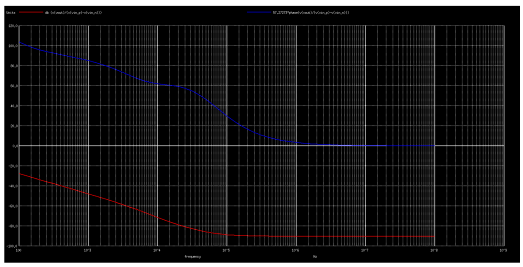

Figure 2: Implemented waveform.

References

[1]

[2] S. A. M. C. M. I. F. A. . A. M. D. M. I. Idris, N. Yusop. Low power operational amplifier in 0.13um technology. Published by Canadian Center of Science and Education, Modern Applied Science; Vol. 9, No. 1; 2015: ResearchGate Link: https://www.researchgate.net/publication/283524419_Low_Power.