Operational Amplifier

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Abstract

This paper describes the analysis and design of a 2-stage CMOS operational amplifier (Op-Amp). The designed circuit operates at 1.8 V of the supply voltage. The supply voltage is scaled down to reduce the power dissipation of the op-amp. This is because the power will be high when there is a large supply voltage. The sky130nm CMOS technology is used to build circuits. The performance parameters such as Gain, Gain Bandwidth Product (GBW), Input Common-Mode Range (ICMR), Slew Rate, etc. also have been analyzed after stimulation, which is carried out using eSim Tool. Obtained results also agree with theoretical predictions and the circuit diagram, waveforms are given in the paper.

1 Circuit Details

Operational Amplifiers are the most useful electronic devices these days, used drastically for signal conditioning, filtering, and the execution of mathematical operations. An operational Amplifier is basically a differential amplifier and the output signal is nothing however difference between the two input signals implemented at the high output impedance. Two-stage Operational Amplifier comprised of three subsections which were a differential gain stage, gain stage, and bias strings. The first stage which was the differential stage of the circuit provided a higher gain while the second stage which was known as the gain stage helped to provide an additional gain to obtain a large output swing. The figure shows the schematic of the two-stage CMOS Operational Amplifier that will be designed through this project using sky130nm technology. The primary phase of the Operational Amplifier is a differential amplifier made up of transistors M1, M2, M3, and M4. This is basically a current mirror (CM) with the active type of load utilized here has three particular preferences. The second stage is used to deliver high gain to the amplifier and is made up of transistors M5 and M6. The biasing circuit stage of the amplifier is accomplished with transistors M5, M6, M7, and M8. Process = 0.13 um Leff = 0.35 um VDD = 1.8 V VSS = 0 V Slew Rate = 20 V/usec Product of gain and bandwidth (GB) = 8.5 MHz Load capacitance = 2 pF ICMR + Vin (max) = 2.7 V ICMR – Vin (min) = 0.8v

2 Implemented Circuit

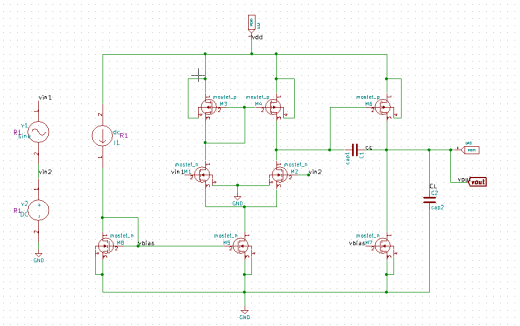

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

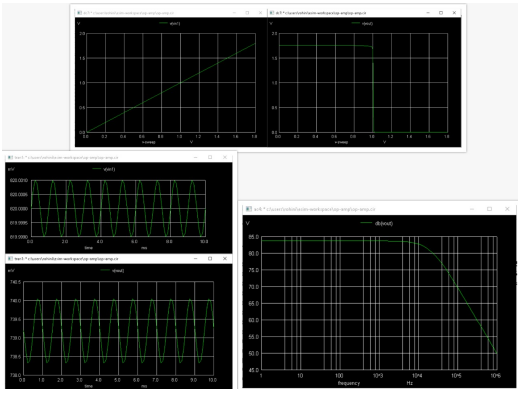

Figure 2: Implemented waveform.

References

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