CMOS Differential cascade voltage switch logic(DCVSL) XOR-XNOR

Krishnamoorthy R, SRM Easwari engineering college

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Abstract

This paper is the study of differential cascade voltage switch logic DCVSL that helps in building better loads for static CMOS designs. It mainly focuses on the XOR XNOR DCVSL circuit design by including the skywater 130nm technology. The advantage of having differential or complimentary outputs that are simultaneously available by eliminating the need of using an inverter that would have an impact on the critical timing path. This circuit has better power dissipation characteristics when compared to its preceding ratioed logic style by eliminating static currents and providing a rail to rail swing. It is observed that the DCVSL reduces the number of gates by a factor of two.
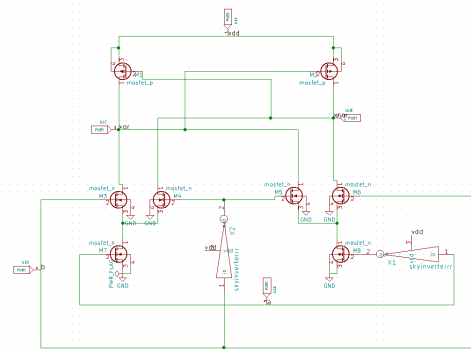
1 Circuit Details

When the differential pairs of MOSFET devices are cascaded into strong combinational logical tree networks, then we can achieve a design leverage in CVSL which is within a single circuit delay and is capable of implementing complex Boolean logic. A DCVS Logic is based on 2 to 1 Multiplexer which is used as an important element in many various circuit designs such as implementation of memory circuits and FPGA. A differential gate requires that each input is provided in a complementary format, and it produces complementary output in return. The feedback mechanism ensures that the load is turned off when it is not needed gives rise to the DCVSL family in CMOS circuits. The circuit uses 2 static PMOS in the pull up network. The pull down networks PDN1 and PDN2 are built using NMOS and are mutually exclusive. The PDN networks are connected as the inputs to the PMOS in a crossed manner. In general, the PMOS devices are deemed to be active low devices i.e conducts when given low voltage and NMOS being active high devices i.e conducts when given high voltage. The low GND and high VDD voltages that are supplied are mapped to the binary 0 and 1. When inputs are given to the a and b terminals, the actual and complementary values are taken. There is only one PDN active at the same time considering the logic. The PDN that is not active is isolated from the VDD and the ground. This circuit can further be used in adder and multiplier circuits. The outputs of the xor and xnor gates are obtained simultaneously.
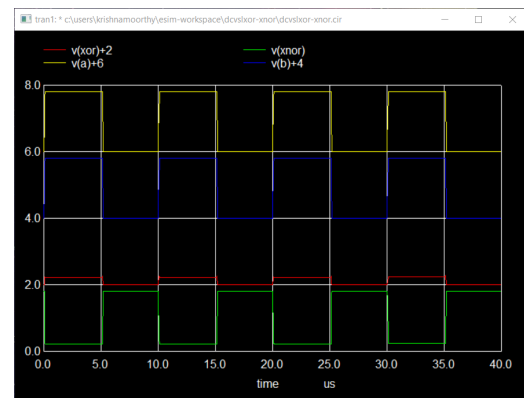
2 Implemented Circuit

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

Figure 2: Implemented waveform.

References

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