

# D FLIP FLOP USING TRANSMISSION GATES

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## Abstract

This paper demonstrates the design and simulation of the D flip flop made up of the transmission gates which will work at the positive edge of the clock pulse. It will store the data present at the input Dinput when the positive clock edge arrives. The D flip flop is the basic element used in the storage of data and is the fundamental block which is used to make bigger circuits. It can also be used to provide delay in the circuits without changing the incoming signal to it. Transmission gates allow the passing of both strong 1 and strong 0, therefore is used here to make the D flip flop. The circuit is designed in 130nm CMOS technology using SkyWater's PDK.

## 2 Implemented Circuit

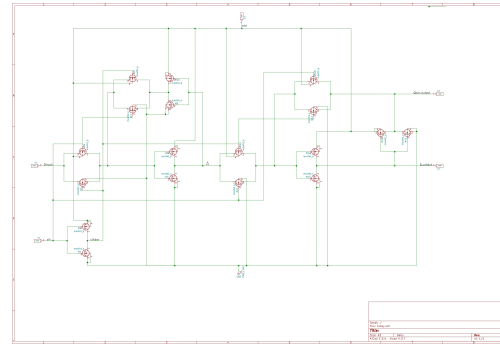


Figure 1: Implemented circuit diagram.

## 3 Implemented Waveforms

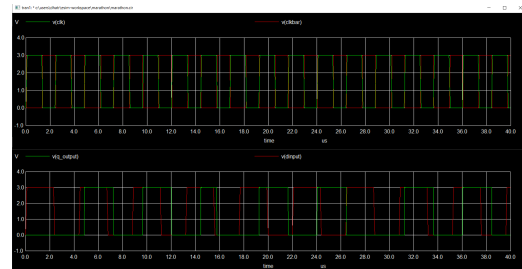


Figure 2: Implemented waveform.

## 1 Circuit Details

The circuit consists of 4 transmission and 4 not gates which are made using the CMOS logic. Total 18 MOSFETs have been used to build this circuit. Sixteen MOSFETs are used to have a Master Slave operation to make the edge triggering possible and the remaining two MOSFETs are used to make an inverter to provide the clkbar(inverted clock signal) from the clk input to control the transmission gates. Let the 4 transmission gates starting from the left be numbered from T1 to T4. The Dinput is the data input pin and the clk is the clock input pin. The 2 output pins are labelled as Q\_output and Qbar\_output(complement of Q) . The two feedback loops are connected in a master-slave structure making the edge triggering possible. When the clk is at logic level 1, T1 and T4 go into the high impedance state thereby not changing the value of the output i.e Q=previous value. When clk becomes 0 the T2 and T3 go into the high impedance state therefore the point A = D'(complement of D). Now when the clk will be transitioning from 0 to 1 the T3 will become on and the value at A will get passed through it making the output Q=D . Now the same process repeats and thereby our circuit behaves like a positive edge triggered D flip flop. The circuit is made using the KiCad (bundled with eSim) software and the simulation is done using ngspice by including the models of the MOSFETs from the SkyWater's PDK. Various combinations of the W/L ratio for the transistors were tried to get the correct output with minimum distortion.

## References

- [1] K. Deignan. Lab project - ee 421l.  
<http://cmosedu.com/jbaker/courses/ee421L/f16/students/deignank/pro>