CMOS Design of 2:1 Multiplexer Using Complementary Pass Transistor log

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Abstract

in this simulation, we simulate the CMOS Design of 2:1 Multiplexer Using Complementary Pass Transistor logic and analyze the timing diagram. The most widely-used solution to deal with the voltage-drop problem is the use of transmission gates. It builds on the complementary properties of NMOS and PMOS transistors: NMOS devices pass a strong 0 but a weak 1, while PMOS transistors pass a strong 1 but a weak 0. The ideal approach is to use an NMOS to pull down and a PMOS to pull up. The transmission gate combines the best of both device flavors by placing an NMOS device in parallel with a PMOS device. The control signals to the transmission gate select and select are complementary.

1 Circuit Details

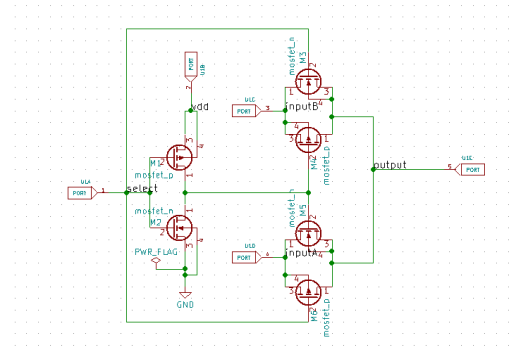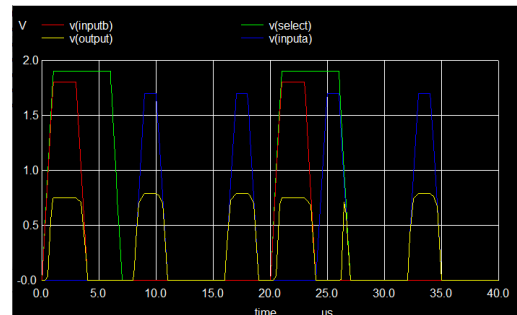This gate selects either input A or B on the basis of the value of the control signal 'select in1'.When control signal select in1 is logic low the output is equal to the input A and when control signal select in1 is logic high the output is equal to the input B. When the control signal select in1 is low then the upper transmission gate turns OFF and it will not allow B to pass through it, At the same time, the lower transmission gate is 'ON' and it allows A to pass through it so the output = A. and when the control signal select in1 is high then the upper transmission gate turns on and it will allow passing B through it, at the same time the lower transmission the gate is turned off and it will not allow A pass-through so the output =B. in this circuit design, the 2:1 multiplexer made by using a two pass Transmission Gate and one inverter. the transmission gate is Two MOS transistors are connected back-to-back in parallel with an inverter used between the gate of the NMOS and PMOS to provide the two complementary control voltages. When the input control signal is LOW, both the NMOS and PMOS transistors are cut off and the switch is open. When the control signal is high, both devices are biased into conduction and the switch is closed. Thus the transmission gate acts as a "closed" switch when control = 1, while the gate acts as an "open" switch when control signal = 0 operating as a voltage-controlled switch.

2 Implemented Circuit

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

Figure 2: Implemented waveform.

References

[1] R. M. R. M. Diwaker Pant, Ankita Pandey. Cmos design of 2:1 multiplexer using complementary pass transistor logic. https://www.researchgate.net/publication/308113538_CMOS_Design