Half Adder

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Abstract

Adders are the digital circuits present in processors in Arithmetic Logic Unit or ALU which play important role in calculation of addresses, table indices and many more similar operations. Adders are constructed for addition of various number systems like decimal, binary, excess 3 and others. However most common adders are binary adders. Half adders are frequently required in VLSI and other fields. Half adders add two single binary digits .Here 1-bit half adder is designed using CMOS. Here circuit is designed has two inputs A,B and Two outputs namely sum and carry. The circuit is designed using esim. The maximum voltage supplied to circuit is VDD and minimum is VSS which is ground voltage.

1 Circuit Details

A combinational circuit is the digital logic circuit in which output depends only on the combination of inputs at that point of time. Half adder is the simplest combinational circuit. Half adder is the simple four terminal device which performs the addition of 2 single binary digits. Half adder has two inputs A, B and two outputs namely sum and carry. Sum is the addition of A and B bits, Carry is the overflow after the addition of bits. The equations of sum and carry are written using truth table, then is simplified by double complimenting the equations and then the circuit is designed using simplified equations of sum and carry with CMOS logic. CMOS is complementary metal oxide semiconductor in which equal number of pmos and nmos are used which means number of pmos equals number of nmos used in the circuit. Equations of sum and carry are simplified by double complimenting and solving one complement since output of CMOS circuits is complemented. The circuit is designed using nmos and pmos directly instead of constructing basics gates and then implementing half adder with them. The circuit is designed using esim. The maximum voltage supplied to circuit is VDD and minimum is VSS which is ground voltage. The circuit diagram and wave forms are shown in the figures below. The circuit design is verified by comparing the expected and generated waveforms.

2 Implemented Circuit

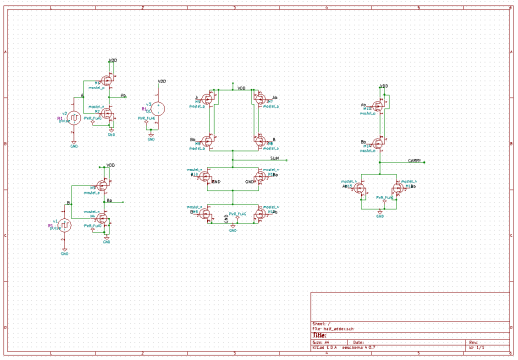

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

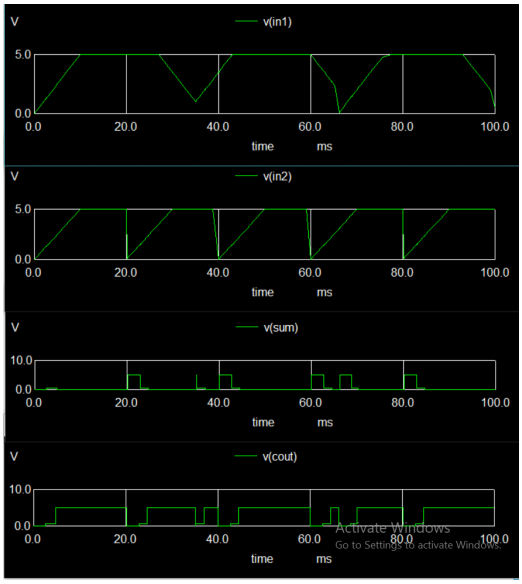

Figure 2: Implemented waveform.

References

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