Phase Frequency Detector for Phase locked loops

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Abstract

This project aims to implement a CMOS based Phase-Frequency detector circuit. Such designs are often a part of Phase locked loops in modern System on Chip units to generate a clock signal with precise frequency. The circuit accepts two inputs. One of them is for reference signal and the other from the feedback loop of the PLL. It outputs a signal which encodes the difference in frequency and phase of the two input signals, which is used as a measure of error in the control system. The circuit features two D type flip flops and an AND gate. A charge pump is often used in the output. The circuit will be designed and verified with eSim EDA tool and will be implemented using SkyWater 130nm PDK technology.

1 Circuit Details

A phase locked loop or PLL in short, is a negative feedback system containing a voltage controlled oscillator and a phase comparator connected such that the oscillator maintains a constant phase angle relative to a reference input signal. PLL can be used to generate stable high frequency signals as output from a fixed low frequency input signal. Such circuits are used in many SoC based systems and are used to clock the microcontrollers and microprocessors by generating a clock signal with precise frequency. A typical PLL uses a phase frequency detector circuit to get a measure of error between the input signal and required signal i.e. it is used to compare the signal from the feedback loop with the input signal. The circuit is idealized when the inputs are frequency locked and phase locked. Two inputs are given to the circuit. Consider a case when an input is higher in frequency than the other. The flip flops are set and reset accordingly. This causes one of the two outputs to spend more of its time in high state than the other. Such behaviour will be carried forward in the PLL to correct the output and to minimize the variation in frequencies. The corresponding reference circuit features a phase frequency detector. Each of the two D flip flops and the AND gate will be implemented using CMOS logic in SkyWater 130nm PDK technology.

2 Implemented Circuit

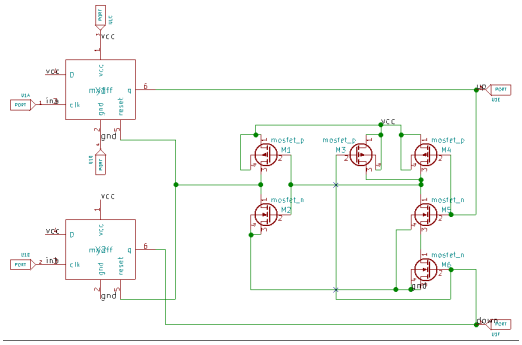

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

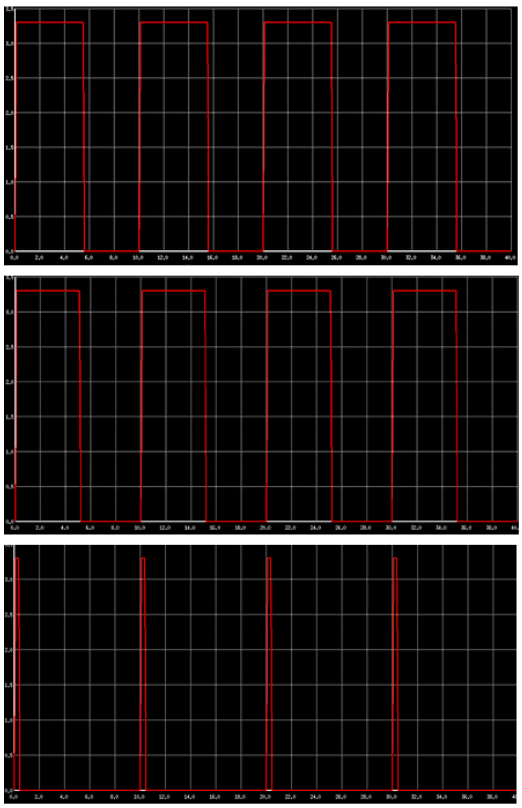

Figure 2: Implemented waveform.

References

[1] A. M. Fahim. Clock generators for soc processors. https://www.springer.com/gp/book/9781402080791.