3T DRAM Cell

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Abstract

DRAM is a type of random access memory that stores bits of data in memory cells comprising MOS transistors and capacitors. DRAM has advantages over SRAM such as higher density at lower costs, low power consumption and usage of lesser transistors per bits of memory storage. Some common DRAM cells designs are 1T1C, 3T, 4T, and 3T1D. In a 3T DRAM cell, there is no constraint on device ratios and the read operation is nondestructive. In addition, the 3T scheme occupies lesser area than the 4T scheme. In a 3T cell, when write line is enabled, data is fed into the cell and stored in a capacitor. When read line is enabled, data is read through the bit line.

1 Circuit Details

A 3T DRAM cell circuit was designed on the open-source tool, eSim based on the 130nm technology node using Google Skywater130 PDK. The schematic was prepared using KiCad and circuit simulation was carried out on ngspice. The circuit, which was designed using P. Asthana et. al. as the base paper, consists of a total of six MOS transistors. Three NMOS transistors M1, M2, and M3 form the DRAM core, one PMOS, M3 enables precharging, and M5 and M6 form the inverter which provides the bit read output. The word line write, WR is fed to the gate of M1 transistor and the word line read, RD is fed to the gate of the M3 transistor. When WR is 1 and RD is 0, that is, during the write operation M1 is on and M2 and M3 are off. The bit write line is fed to M1. If the bit value is 1, then Vdd minus Vth is stored at the storage node, vout. If the bit value is 0, then the value stored is 0. When WR is 0 and RD is 1, that is, during the read operation, M1 is off and M3 is on. If vout initially stored Vdd minus Vth then now, M2 will be on. Then, bit read line tends to 0. To put it simply, when the WR line is enabled, bit write line inputs bits into the memory cell which get written at the storage node, vout. When RD line is enabled, bit read line outputs the bit value that was stored during the write operation. Various voltage inputs have been appropriately considered as pulse signals or DC signals using P.Asthana et. al. as the reference paper.

2 Implemented Circuit

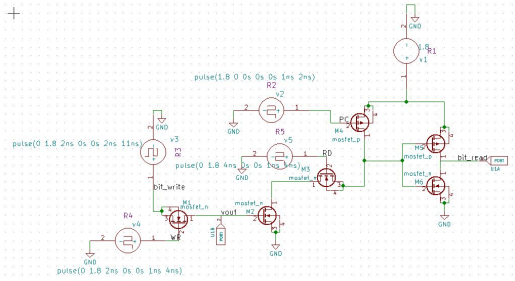

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

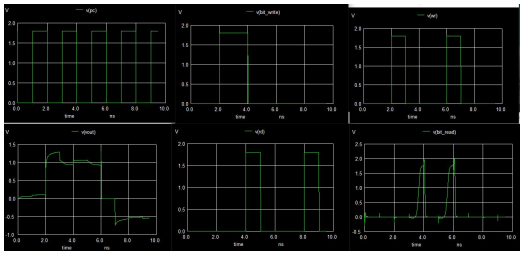

Figure 2: Implemented waveform.

References

[1] P. A. S. Mangesh. Performance comparison of 4t, 3t and 3t1d dram cell design on 32 nm technology. https://www.researchgate.net/publication/276200666_Design_and_In

[2] S. A. A. M. S. B. Singh. Analysis of power in 3t dram and 4t dram cell design for different technology. https://ieeexplore.ieee.org/document/6409043.