Design and Analysis of DIBO Differential Amplifier

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Abstract

The paper describes the design and analysis of Differential Input Balanced Output (DIBO) differential amplifier. The amplifier is the basic building block of analog circuit design. The circuit is designed for a threshold voltage of 1V and differential gain of Ad=2.965. This amplifier, amplifiers the difference of the two inputs. The noise present in the input signal can be eliminated by this amplifier. The amplifier rejects the common mode signal. The amplifier provides immunity to noise. The differential amplifier is simulated using eSim and 130nm Skywater technology. The obtained output waveforms shown the gain achieved.

1 Circuit Details

The differential amplifier is a commonly used circuit in analog design. The Differential amplifies the difference of the two input voltages by the constant differential gain Ad. If a part of the input is common to both the inputs, the differential amplifier rejects the difference. This common difference is called as common mode rejection. The design uses two input signals and hence called as dual input. It is balanced output because the output taken at both the drains are at same potential with respect to ground. Figure 1 shows the design of differential amplifier. Inputs Vin1 and Vin2 are applied to the gate of M1 and M2. These two inputs are same in magnitude and opposite in phase. The differential output is measured between the two drain of M1 and M2. Two identical registers Rd1 and Rd2 are connected to drain of MOSFETs used as load puts the transistor in saturation. The design is simulated in esim using 130nm skywater technology. This technology is developed by Cypress semiconductor. It is open source a foundry technology. Design: The design of MOSFET differential amplifier is as shown in below equations Given Rd1=Rd2=25Kohms, VDD=5V, VSS=-5V, VTN1=VTN2=1V, kn1=kn2=50uA/Vsquare. By DC Analysis VGSQ=VSS-2IdqRs Idq=kn(VGSQVTN) square Substituting and Solving the above two equation VGSQ=2.186v=VGSQ1=VGSQ2 ID=70.33uA gm=2kn(VGS-VTN)=0.1186uA Differential gain Ad=gm RD =2.965 Figure 2 shows the differential amplifier designed for gain of 2.965 is achieved.

2 Implemented Circuit

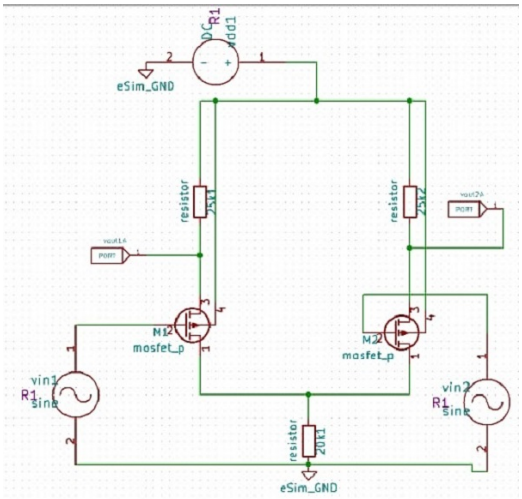

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

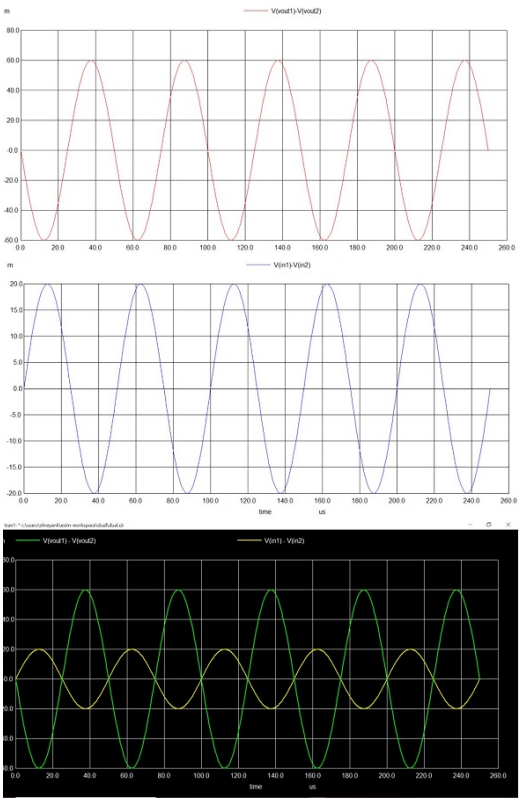

Figure 2: Implemented waveform.

References

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