Low power and High speed 1 bit full adder circuit

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Abstract

Microprocessors, microcontrollers, memory chips and other digital logic circuits are all built using CMOS technology. High noise immunity and low static power consumption are two significant properties of CMOS electronics. This work describes a SERF which is a 1 bit full adder cell that uses ten CMOS transistor with four T XOR logics to achieve low power and fast speed. These designs are aimed at minimizing power dissipation and transistor count while also reducing propagation delay. To achieve a small circuit design, the suggested full adder circuit use ten transistors. The suggested circuit was tested using the eSim Circuit Design and Simulation and skywater 130 nm technology.
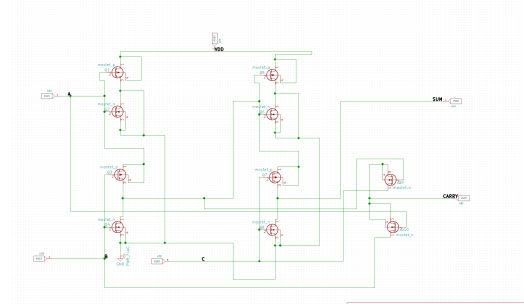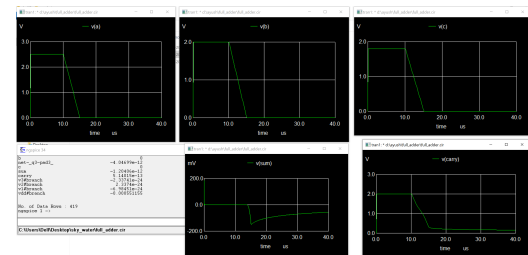
1 Circuit Details

Many applications like DSP architectures which are application specific and microprocessors have been widely used in many VLSI Systems. In most of these systems, the adder is a component of the Critique, which defines the systems overall performance. As a result, enhancing the performance of the one bit adder cell is a critical objective as Due to the rapid rise of technologies in mobile communication and computing, the construction of low-power VLSI systems has recently acquired traction. Battery technology, on the other hands not growing as quickly as microelectronics technology. However, the amount of energy available to mobile systems is restricted . As a result, designers are faced with increased constraints, such as high speed, high performance, tiny silicon area, and low power consumption. So, in today's VLSI world, developing a low-power, high performance adder cell is essential. This adder is made up of ten CMOS transistors with a 4T XOR logics. This design is known as a low-power adder since it does not have a direct link to the ground and can re-apply the load charge to the control gate, which is why it is also known as a Static energy recovery complete adder . The design technique takes three inputs and produces two sum and carry outputs. The low power consumption of this circuit is a benefitted in small area and less PDP compare to pass transistor logic (PTL).

2 Implemented Circuit

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

Figure 2: Implemented waveform.

References

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