Design and Analysis of a 2-input NAND Gate in 130 nm CMOS Technology

Soham Sen, Amity University Kolkata

July 30, 2021

Abstract

The paper constitutes the design and analysis of a 2 input Complementary MOS NAND gate. NAND gate is one of the essential logic gates to perform the digital operation on the input signals. It is the mixture of AND gate circuit followed by NOT gate that is it is the opposite operation of AND gate circuit where the logic NAND gate circuit is complementary of AND gate circuit. The logic output of the NAND gate is high when either of the inputs is low. The logic output of the NAND gate circuit is low only when the inputs are high. The 2 input NAND gate has been designed using 130nm CMOS Technology.
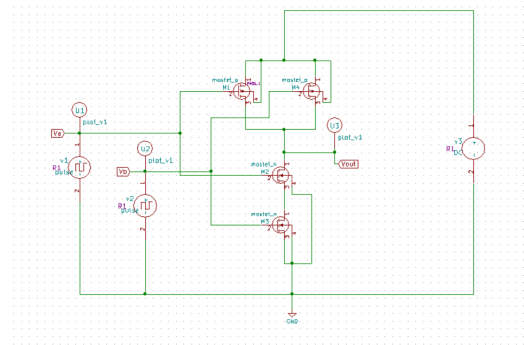
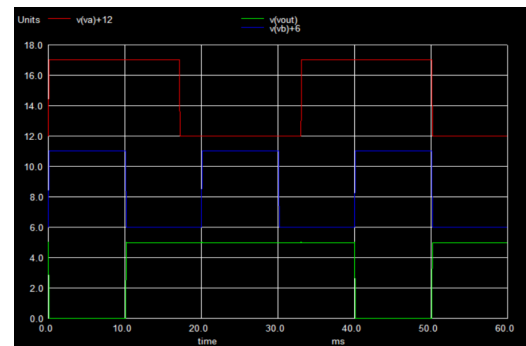## 1 Circuit Details

Logic gates perform basic logical functions and are the elemental building blocks of digital integrated circuits. Most logic gates take an input of two binary values, and output one value of a 1 or 0. NAND circuit is one of the important logic gates.CMOS is the combination of PMOS and NMOS. Figure 1 shows the realization of a 2 input CMOS NAND gate. It consists of two series NMOS transistors between Vout and GND and two parallel PMOS transistors between Vout and Vdd i.e. at 5V. If both inputs Va and Vb are low i.e. at 0V, both of the NMOS transistors will be OFF and both of the PMOS transistors will be ON. Hence, the output Vout will be high i.e. 5V. If any one of the inputs is high i.e at 5V and the other input is low i.e at 0V, one of the NMOS transistors will be ON and one among the two parallel PMOS transistors will be ON, creating a path from Vout to Vdd. Hence, the output Vout will be high i.e. at 5V. If both inputs are high i.e. 5V, both of the NMOS transistors will be ON and both of the PMOS transistors will be OFF. Hence, the output will be low i.e at 0V. When any of the inputs are low, then the output is pulled high through the parallel PMOS transistors. When all of the inputs are high, then the output is pulled low through the series NMOS transistors. If we apply 2 different clock signals as the inputs of NAND gate Va and Vb, then the output of the NAND gate is shown in Figure 2 where Va, Vb are inputs and Vout is output.

2 Implemented Circuit

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

Figure 2: Implemented waveform.

References

[1] Cmos gate circuitry. https://cutt.ly/xnNZHeh.

[2] S. Kar. Cmos nand gate using 0.5um technology. https://cutt.ly/QnNnCXa.

[3] N. H. E. Weste. Cmos vlsi design : A circuits and systems perspective. https://cutt.ly/InNnZPb.