

Circuit-Level Modelling and Verification of a Wiegand Pulse-Based Communication Interface Using eSim

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Screening Task: FOSSEE eSim – Task 2: Communication Protocol Modelling and Verification

Objective

To design, model, and verify an 8-bit Wiegand pulse-based communication interface using eSim, and to analyse its transmitter and receiver operation through ngspice transient simulation and Python-based waveform visualization.

Specific Objectives

- To model an 8-bit parallel-in/serial-out data transmission system for Wiegand communication.
- To generate D0 and D1 active-low pulses corresponding to binary 0 and 1, respectively.
- To analyse the operation of the transmitter and receiver sections at circuit level.
- To verify the transmission of the test data 10110101 using ngspice waveforms.
- To visualize and validate the simulated Wiegand signals using Python plots.
- To study the timing, pulse polarity, and signal characteristics of the Wiegand interface.

Theory / Description

The Wiegand interface is a reliable pulse-based communication technique widely used in access-control and identification systems. Unlike conventional serial communication protocols, Wiegand transmission represents binary information using two dedicated signal lines: **D0** and **D1**. An active-low pulse on the D0 line represents a binary **0**, whereas an active-low pulse on the D1 line represents a binary **1**. This distinctive pulse-based mechanism enables simple and robust transmission of digital information.

In this project, an **8-bit Wiegand communication interface** is designed, modelled, and verified using **eSim** and its integrated **ngspice** simulation environment. An 8-bit parallel input sequence **10110101** is applied to a parallel-in/serial-out shift register. The stored data is converted into a serial bit stream and used to control transistor-based low-side drivers for generating the corresponding D0 and D1 Wiegand pulses. An optocoupler-based receiver section is incorporated to provide electrical isolation and detect the transmitted pulse signals. The circuit behaviour is analysed through transient simulation to verify the timing, polarity, and correspondence of the generated Wiegand pulses with the applied digital data.

Circuit Diagram(s)

[illegible]

Figure 2: Wiegand Receiver Circuit Implemented in eSim

Results / Output

The proposed 8-bit Wiegand communication interface was simulated using **eSim** and **ngspice** for the input data sequence **10110101**. The transient simulation produced the expected active-low pulses on the D0 and D1 Wiegand transmission lines. The **D0 line generates pulses corresponding to binary 0**, while the **D1 line generates pulses corresponding to binary 1**. The simulated waveforms were exported and plotted using **Python**, providing a clear representation of the transmitted Wiegand signals. The results demonstrate the correct generation and timing of the D0 and D1 pulses for the applied 8-bit data sequence.

Simulation Outputs

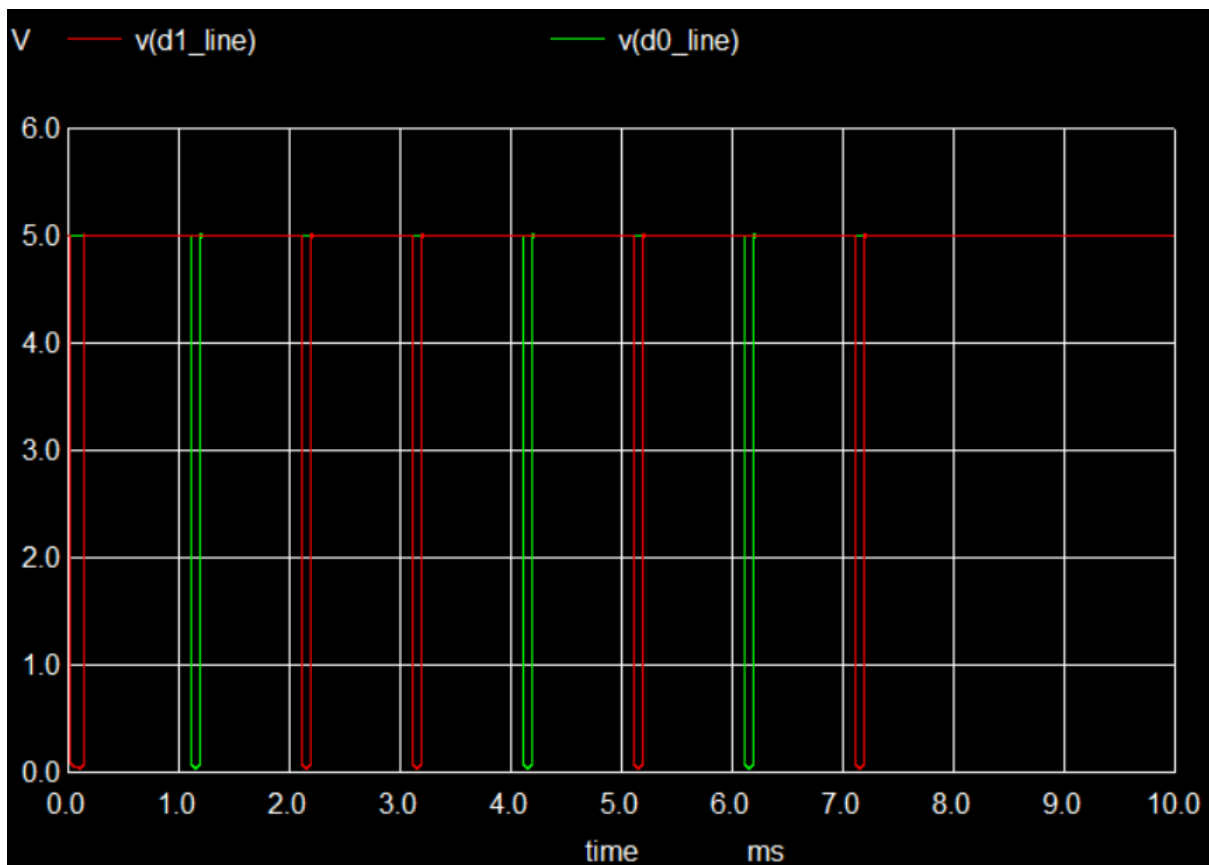


Figure 3: Ngspice Simulation Output of Wiegand D0 and D1 Signals

The simulated Wiegand transmission lines showing the active-low D0 and D1 pulses corresponding to the applied binary sequence 10110101.

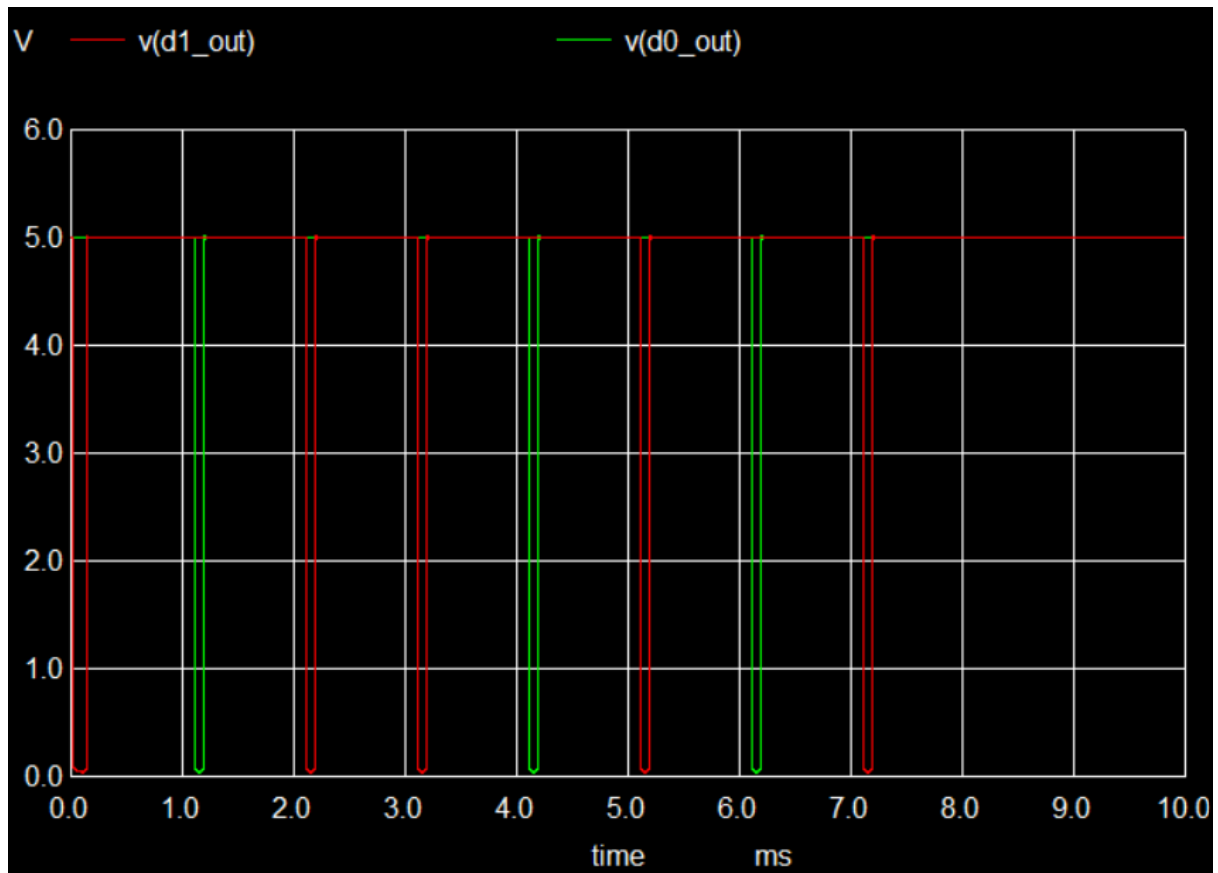


Figure 4: Ngspice Simulation Output of Receiver Signals

The simulated receiver output waveforms corresponding to the detected D0 and D1 Wiegand pulses.

Python Simulation Outputs

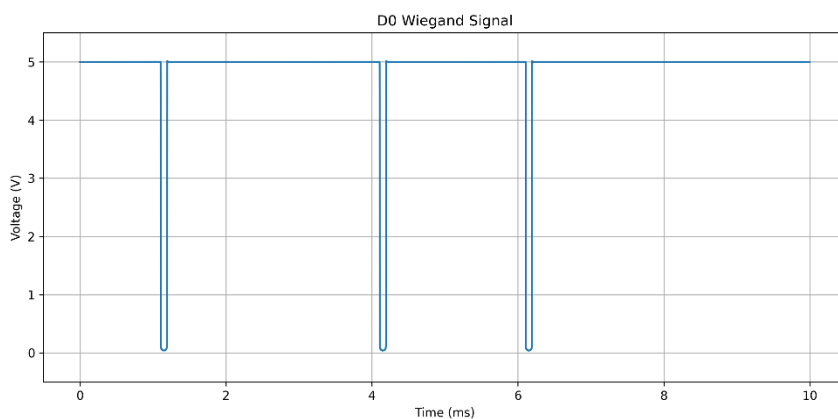


Figure 5: Python Plot of D0 Wiegand Signal

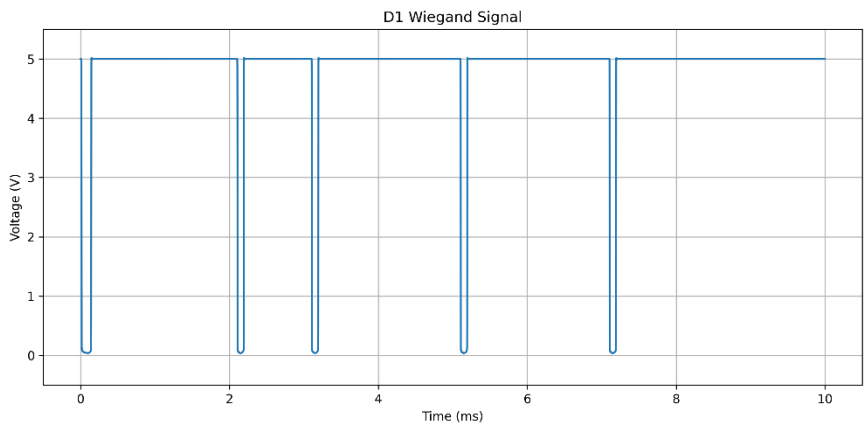


Figure 6: Python Plot of D1 Wiegand Signal

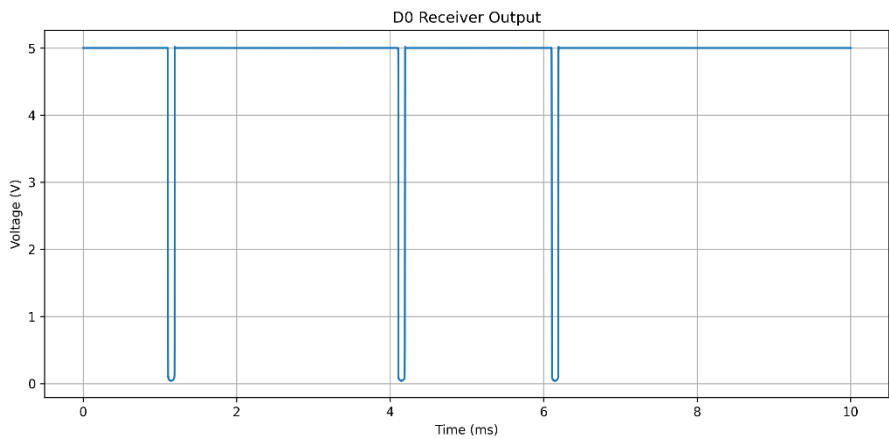


Figure 7: Python Plot of D0 Receiver Output

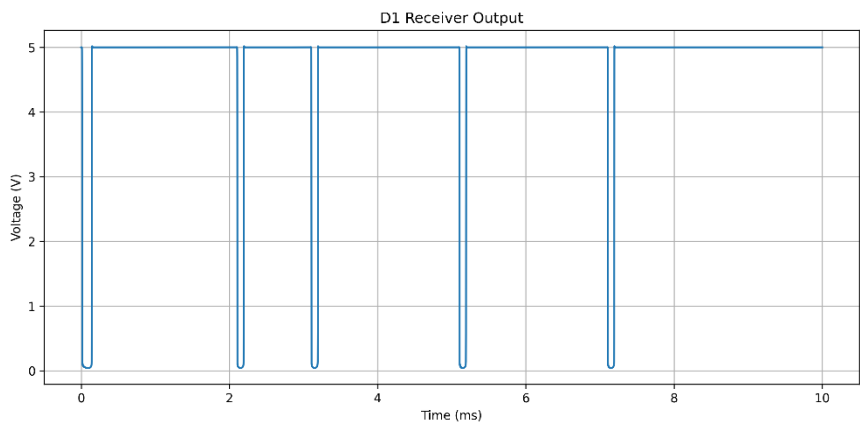


Figure 8: Python Plot of D1 Receiver Output

Observed Output

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WIEGAND PYTHON PLOTS GENERATED
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D0 Wiegand   : Figure_D0_Wiegand.png
D1 Wiegand   : Figure_D1_Wiegand.png
D0 Output    : Figure_D0_Output.png
D1 Output    : Figure_D1_Output.png

Expected input:
BIT7..BIT0 = 10110101

Expected Wiegand pulses:
D0 = 3 pulses
D1 = 5 pulses
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For the applied input sequence:

BIT7 → BIT0 = 10110101

the expected Wiegand transmission consists of:

- Binary 0 → D0 pulse: 3 pulses
- Binary 1 → D1 pulse: 5 pulses
- Total transmitted bits: 8

The ngspice and Python waveforms demonstrate the generation of the corresponding D0 and D1 pulse signals, thereby verifying the basic operation of the Wiegand pulse-based transmitter.

Conclusion

The 8-bit Wiegand pulse-based communication interface was successfully designed and simulated using eSim and ngspice. The applied input sequence 10110101 was converted into the corresponding active-low D0 and D1 Wiegand pulses using the transmitter circuit. The receiver section was designed to detect the transmitted pulses, and the resulting waveforms were analysed through ngspice and Python plots. The obtained results verify the expected pulse-based representation of the input data and demonstrate the practical application of circuit-level modelling and simulation for a Wiegand communication interface.

References

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6. ngspice User Manual — Reference material for circuit-level transient analysis and waveform simulation.