

Circuit Simulation Project

<https://esim.fossee.in/circuit-simulation-project>



The Circuit Simulation Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for designing and simulating electrical and electronic circuits for learning and application purposes. The objective is to create and document original, application-based, or proof-of-concept circuit designs using eSim to build an open-source resource database.

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Title of the circuit : Design and Simulation of Bell 202 FSK Transceiver for Industrial HART Communication Protocol Using eSim

Theory/Description : The Highway Addressable Remote Transducer (HART) communication protocol is an industry-standard mixed-signal communication system widely deployed in process automation and industrial instrumentation. Operating under the Bell 202 Frequency Shift Keying (FSK) physical layer standard, HART transmits asynchronous digital binary data at a standard baud rate of 1200 Baud. In this modulation scheme, digital logic states are represented by distinct sinusoidal carrier frequencies: a logic '1' (Mark frequency) is encoded using a 1200 Hz sinusoidal tone, while a logic '0' (Space frequency) is encoded using a 2200 Hz sinusoidal tone.

The system architecture implemented in this circuit comprises two primary subsystems: a Continuous-Phase FSK Transmitter (Modulator) and an Analog Discriminator Receiver (Demodulator).

1. **Transmitter (Modulator Stage):** The transmitter synthesizes the FSK signal using a multiplexed carrier approach. An incoming digital binary bitstream and its logical complement drive a pair of high-speed analog bilateral switches. These switches alternately route the continuous Mark (1200 Hz) and Space (2200 Hz) sinusoidal sources into a common summing transmission node. This method guarantees smooth phase transitions across symbol boundaries without introducing high-frequency phase discontinuities.
2. **Receiver (Demodulator Stage):** The demodulator extracts and reconstructs the transmitted binary data through a non-coherent frequency discriminator network:
 - **Dual RLC Bandpass Discriminator:** The composite FSK signal is fed simultaneously into two parallel tuned series RLC resonant tank filters. One filter is tuned precisely to resonate at the Mark frequency, while the second filter is tuned to the Space frequency. When a given frequency is present on the line, its corresponding tank achieves minimum impedance and maximum voltage transfer across the load, effectively splitting the mixed FSK carrier into isolated Mark and Space signal paths.

- **Envelope Rectification & Filtering:** Following frequency separation, each channel is routed through a precision half-wave diode envelope detector paired with an RC low-pass filter. The envelope detector extracts the unipolar peak amplitude envelope of the active carrier tone while the parallel discharge network filters out high-frequency carrier ripple, generating continuous differential DC envelope voltages (v_{mark} and v_{space}).
- **Schmitt Trigger Comparator:** The recovered DC envelopes are applied directly to the inverting and non-inverting differential inputs of an operational amplifier acting as a high-gain voltage comparator. A positive feedback network introduces controlled hysteresis (Schmitt trigger configuration) to eliminate false chattering caused by transient switching noise and carrier ripple. The comparator performs rail-to-rail digital slicing, generating a sharp binary output pulse stream that accurately reconstructs the original transmitted digital data bit-for-bit.

Reason to simulate with eSim : Simulating this mixed-signal communication protocol in eSim offers significant engineering and pedagogical value by providing a realistic, component-level simulation environment:

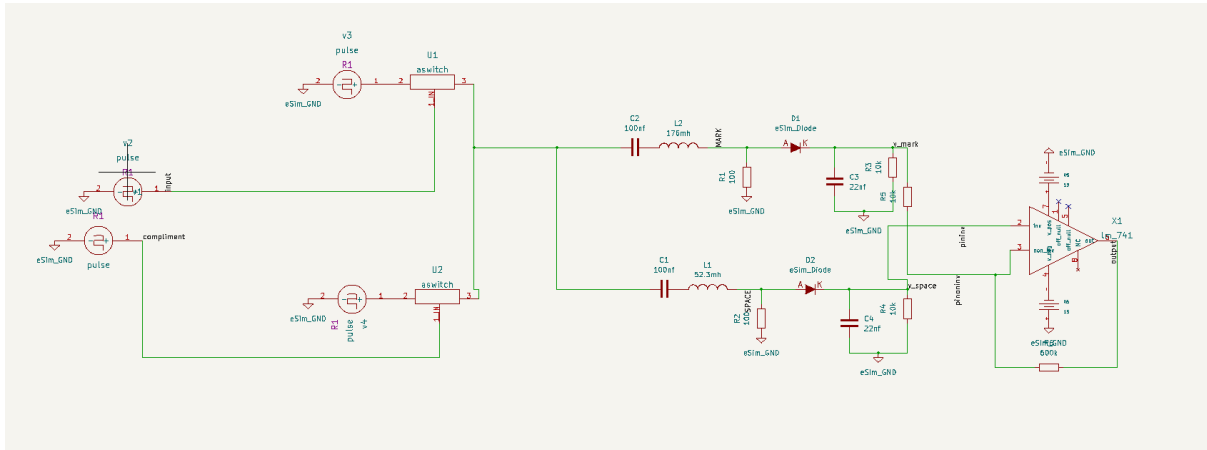
- **True Mixed-Signal Co-Simulation:** eSim provides seamless co-simulation capability between discrete digital switching logic and continuous-time analog LC filtering, rectification, and nonlinear op-amp dynamics.
- **Component-Level Discrete Modeling:** Instead of relying on high-level mathematical black-box blocks, the entire transceiver is built using fundamental passive and active components (inductors, capacitors, diodes, analog switches, and operational amplifiers), closely reflecting physical printed circuit board (PCB) hardware behavior.
- **Filter Dynamics & Transient Analysis:** eSim's Ngspice engine allows precise transient verification of critical analog behavior, including resonant tank Q -factor selectivity, time-domain envelope decay constants, diode turn-on thresholds, and comparator switching delays across bit transitions.

Expected Outcome/outputs :

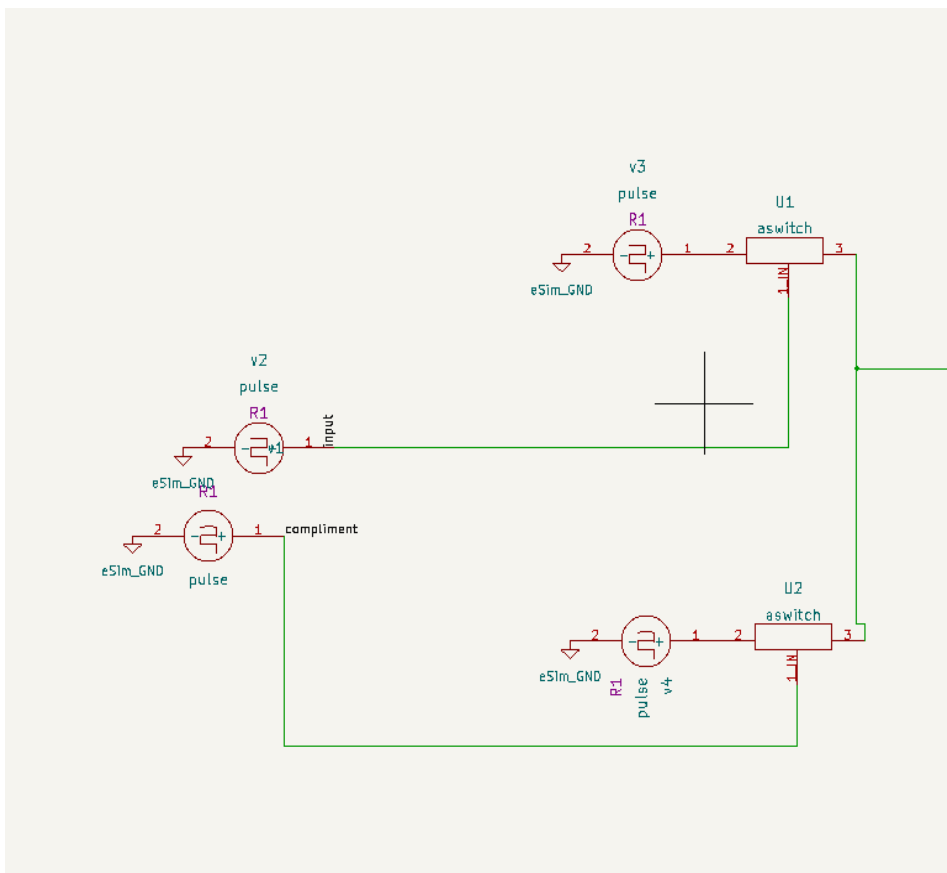
- **Continuous FSK Modulation:** Clean, uninterrupted frequency modulation at the transmitter node, alternating between Mark (1200 Hz) and Space (2200 Hz) sinusoidal tones synchronized with the input bitstream.
- **Dual Frequency Separation:** Selective amplitude peaking at the output of the tuned RLC filters corresponding to the active carrier frequency.
- **Stable Envelope Generation:** Demodulated Mark and Space envelope signals (v_{mark} and v_{space}) exhibiting clear antiphase voltage separation across every bit period.

- **Accurate Digital Data Recovery:** The Schmitt trigger comparator produces a stable, full rail-to-rail digital square wave with matched timing, reproducing the exact sequence and duration of the transmitted digital input pulses.

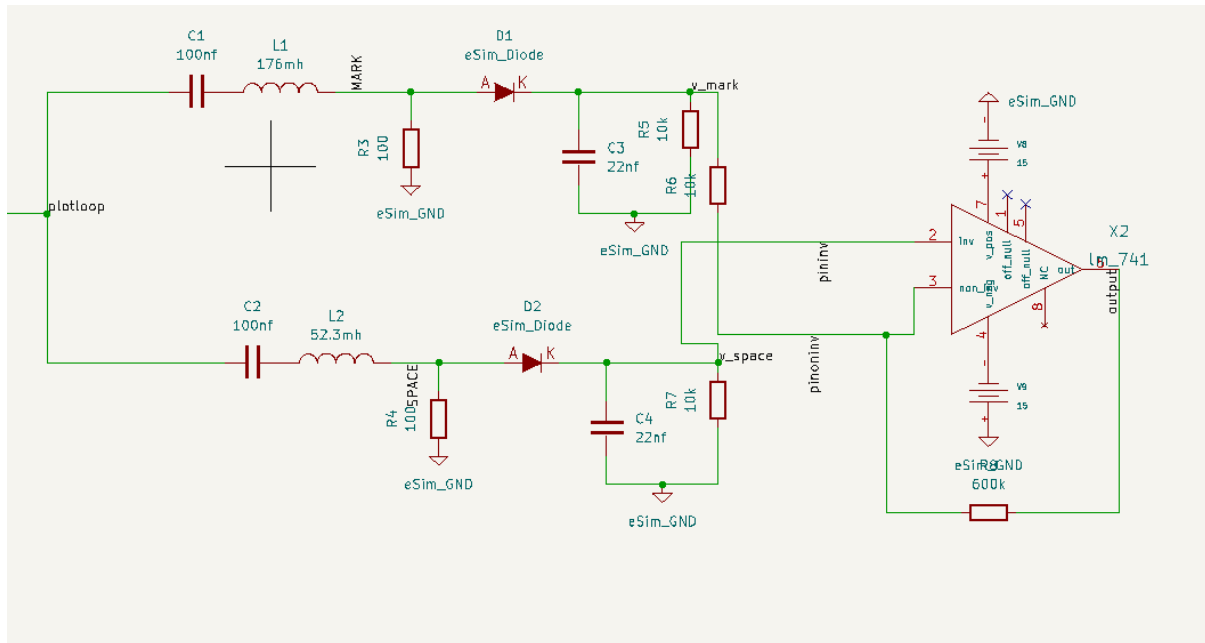
Circuit Diagram(s) :



Transmitter

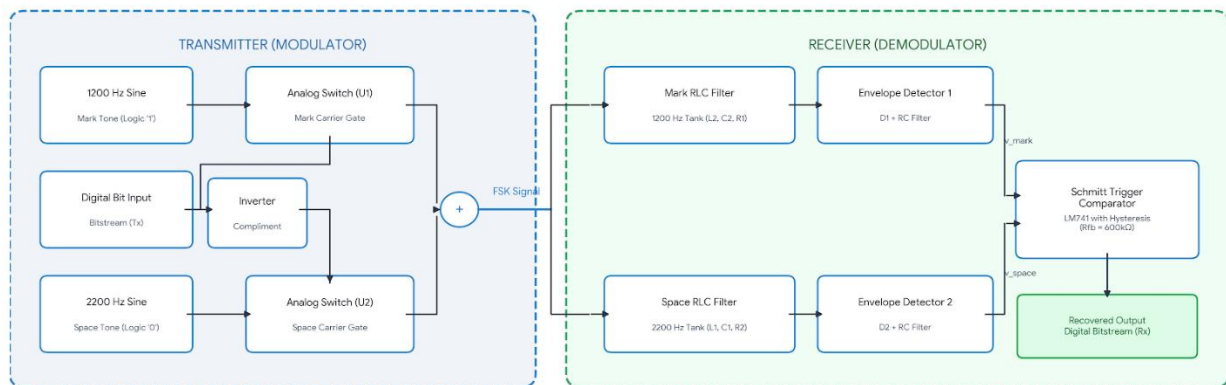


Receiver



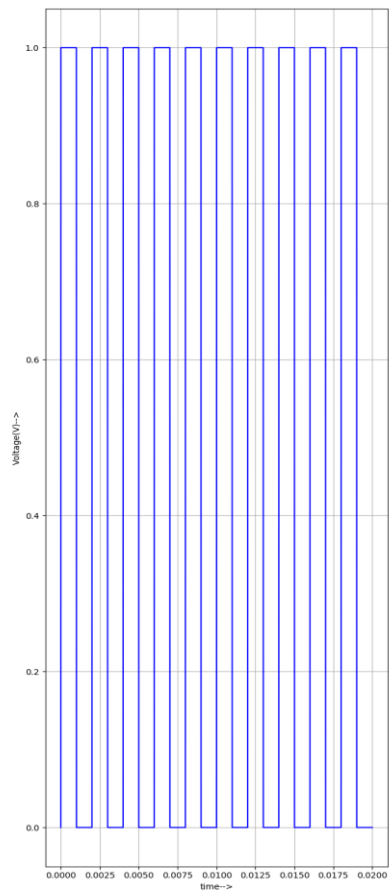
Block Diagram (s) :

HART Protocol Bell 202 FSK Transceiver System Architecture

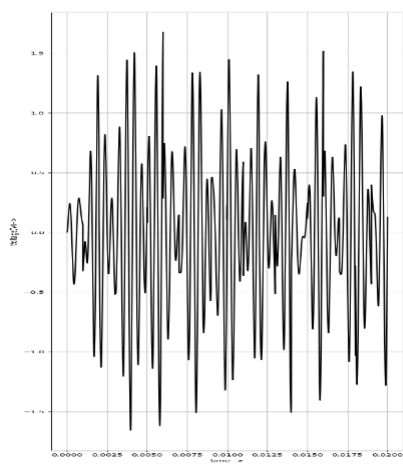


Expected Results (Input, Output waveforms and/or Multimeter readings) :

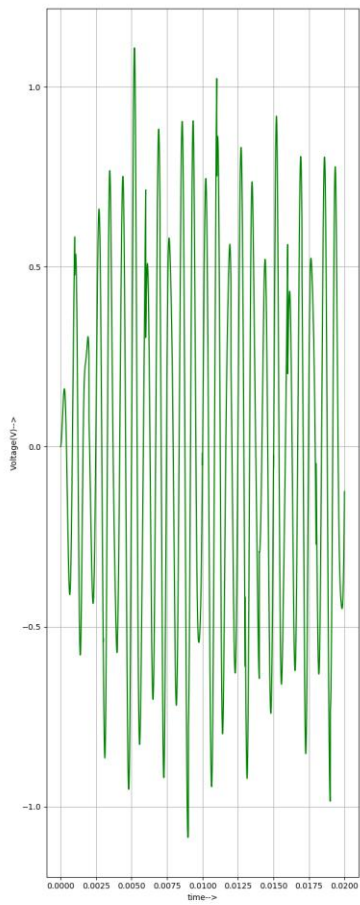
input



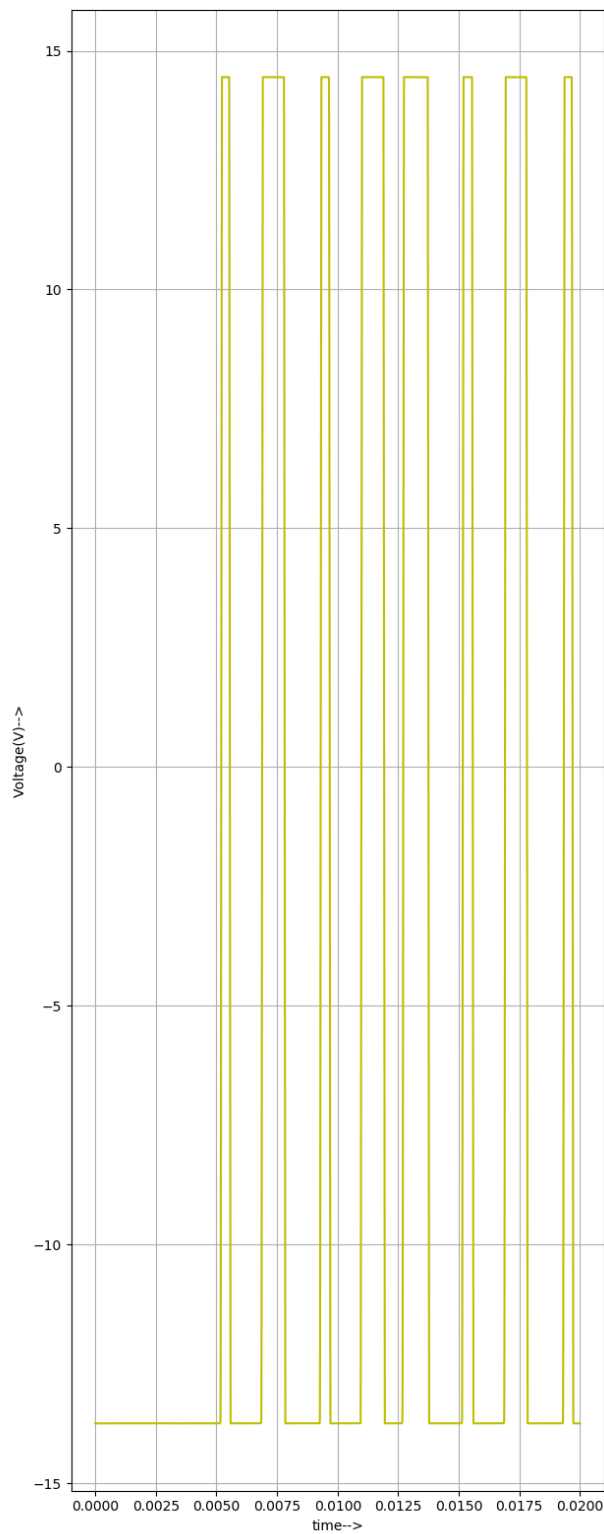
SPACE



MARK



OUTPUT



The incoming mixed FSK signal is separated into its 1200 Hz (Mark) and 2200 Hz (Space) components using parallel tuned series-resonant RLC tank filters. These carrier tones are then converted into DC envelope voltages (v_{mark} and v_{space}) via half-wave diode

envelope detectors with low-pass RC filtering. Finally, an LM741 Schmitt trigger comparator slices the differential envelope voltages with hysteresis to eliminate noise, reconstructing the original 8-bit digital square wave rail-to-rail.

Timing Verification and Transient Response Analysis

- Initial Settling Latency (0--5 ms):
 - High- Q passive LC resonant tanks (176 mH/52.3 mH) require multiple carrier cycles to accumulate reactive energy from a zero initial state.
 - Envelope detector capacitors (22 nF) must overcome the diode forward turn-on threshold ($V_D \approx 0.6\text{--}0.7$ V), holding the comparator at the negative saturation rail until steady-state is achieved.
- Propagation Delay & Group Delay ($\approx 0.3\text{--}0.4$ ms):
 - Frequency discrimination through narrowband RLC bandpass filters introduces inherent group delay ($\tau_g = -\frac{d\phi}{d\omega}$).
 - Envelope detector low-pass filtering ($\tau = RC \approx 0.22$ ms) adds finite exponential rise and decay times before envelope voltages intersect.
- Pulse-Width Jitter / Duty Cycle Distortion:
 - Asymmetrical RC charge (fast via forward-biased diode) and discharge (slower via 10 k Ω shunt resistor) rates create unequal envelope slopes.
 - Schmitt trigger hysteresis thresholds (V_{TH}/V_{TL}) slice these non-vertical edges at slight time offsets, causing minor pulse-width narrowing.
- Synchronization & Bit Recovery:
 - Following the initial 5 ms transient settling window, the demodulator achieves complete symbol synchronization, recovering all 8 transmitted bits bit-for-bit without logic errors.

Research Paper/Journal/etc. : *International Journal of Computing* (abbreviated as *Computing* in the header)

Title : HART Protocol Analyser Based in LabVIEW

Author : (Author names as per publication)

Page No. : 39–42

Link : [HART Protocol Analyser Based in LabVIEW](#)

Source/Reference(s) : [HART Protocol Analyser Based in LabVIEW](#)

- B. P. Lathi & Zhi Ding: *Modern Digital and Analog Communication Systems* (FSK modulation & non-coherent detection theory).

- Tony R. Kuphaldt: *Lessons in Industrial Instrumentation* (HART protocol & Bell 202 FSK standard).
 - Sergio Franco: *Design with Operational Amplifiers and Analog Integrated Circuits* (LC bandpass filters, envelope detectors, & Schmitt triggers).
 - Adel S. Sedra & Kenneth C. Smith: *Microelectronic Circuits* (diode rectification, RC time constants, & comparator switching).
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Note: Fields marked with an asterisk (*) are mandatory and must be filled for successful submission.