

Circuit Simulation Report

Circuit-Level Modelling and Verification of DALI Communication Protocol

Contributor	Sayem Azam	Standard	IEC 60929 / IEC 62386 / Microchip AN1465
Simulation Tool	eSim 2.1 / Ngspice 45.2	Date	April 2026

Abstract

The Digitally Addressable Lighting Interface (DALI) is an internationally standardised two-wire serial communication protocol defined under IEC 60929 and IEC 62386, widely used for digital control of dimmable fluorescent ballasts and lighting systems. This project presents the design and simulation of a DALI protocol transceiver in eSim using Ngspice, implementing Manchester (bi-phase) encoding and decoding at 1200 bps. The transmitter encodes a digital bitstream using NPN transistor switching and drives the DALI bus at correct voltage levels — Logic LOW below 9.5V and Logic HIGH/idle at 16V. The receiver decodes the Manchester-encoded bus signal back to the original bitstream using ADC/DAC bridge subcircuits. Simulation confirms successful Manchester encoding and correct digital recovery at the receiver, verifying the DALI physical layer protocol as specified in Microchip AN1465.

Objective

To design and simulate a complete DALI protocol transceiver at circuit level in eSim, implementing Manchester encoding/decoding, and verifying correct DALI bus signal levels and digital data recovery through transient simulation.

Key Specifications

Parameter	Value	Parameter	Value
Data rate	1200 bps	DALI Logic LOW	< 9.5V (active)
Bit period	833.33 us	DALI Logic HIGH/Idle	16V (9.5V-22.5V)
Half-bit time (Te)	416.67 us	Forward frame	38 Te = 15.83 ms
Encoding	Manchester bi-phase	Supply voltage	16V DC

Simulation Results

Figure 1 shows the Tx_Digital_In signal — a clean 1200 bps square wave at 5V representing the digital input bitstream. The period is 833 us with 50% duty cycle matching the DALI bit time.

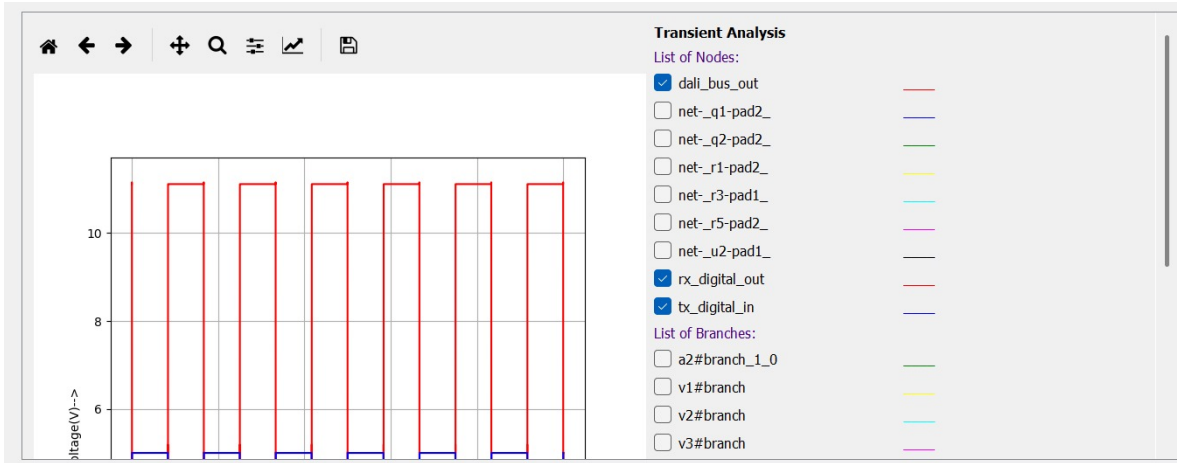


Figure 1: Tx_Digital_In — digital input bitstream at 1200 bps (0V to 5V square wave)

Figure 2 shows the DALI_Bus_Out waveform — the Manchester encoded DALI bus signal. The bus switches between 0V (active LOW, transistor ON) and approximately 11V (idle HIGH), correctly satisfying the DALI

electrical specification of Logic LOW below 9.5V and Logic HIGH between 9.5V and 22.5V.

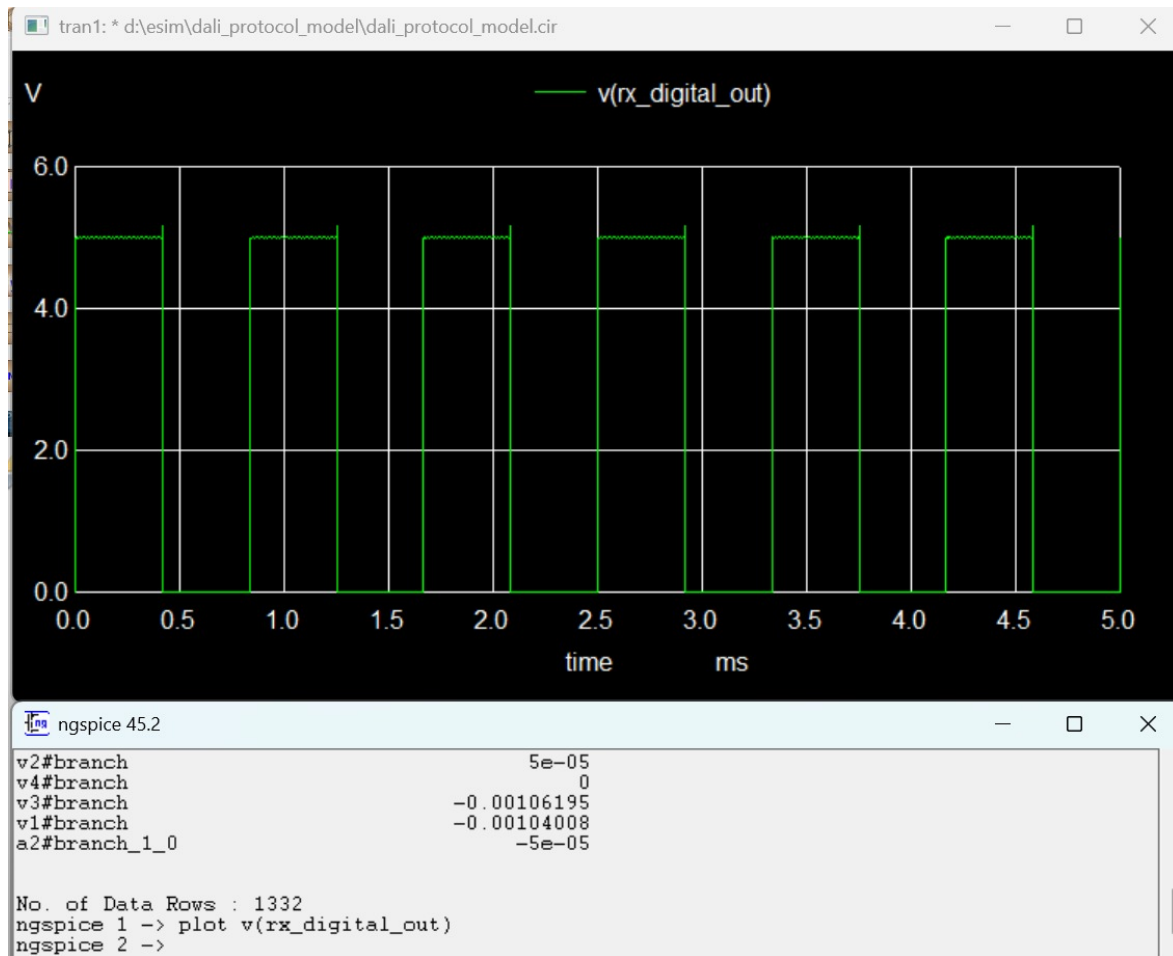


Figure 2: DALI_Bus_Out — Manchester encoded DALI bus waveform (0V to 11V switching)

Figure 3 shows the Rx_Digital_Out — the recovered digital signal at the receiver output. The signal switches cleanly between 0V and 5V, correctly reconstructing the original Tx_Digital_In bitstream, confirming successful Manchester decoding.

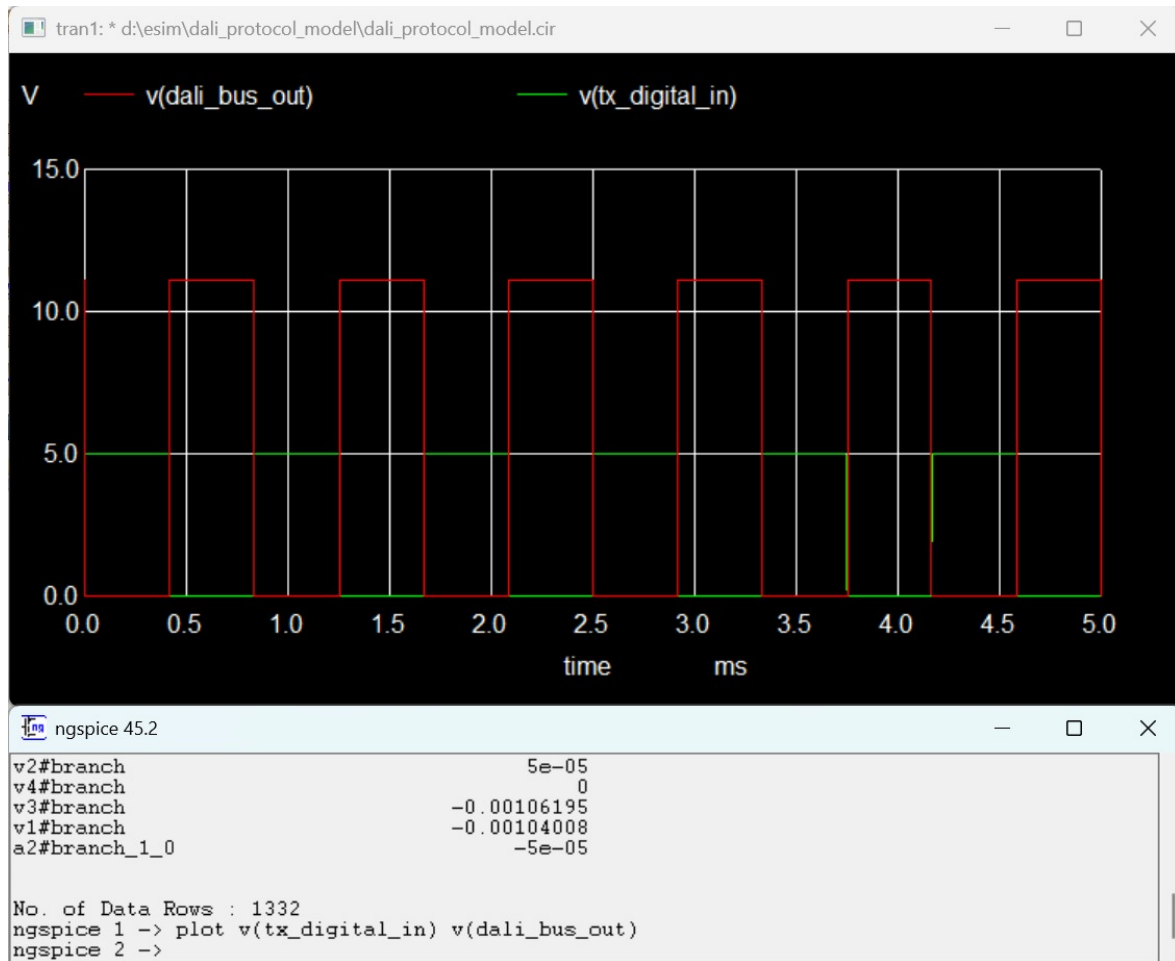


Figure 3: Rx_Digital_Out — recovered digital output confirming correct Manchester decoding

Figure 4 overlays Tx_Digital_In (green, 5V) and DALI_Bus_Out (red, 0-11V). When Tx_Digital_In is HIGH, the NPN transistor turns ON pulling the DALI bus LOW. When Tx_Digital_In is LOW, the transistor turns OFF and the bus returns to HIGH — confirming correct Manchester encoding behaviour.

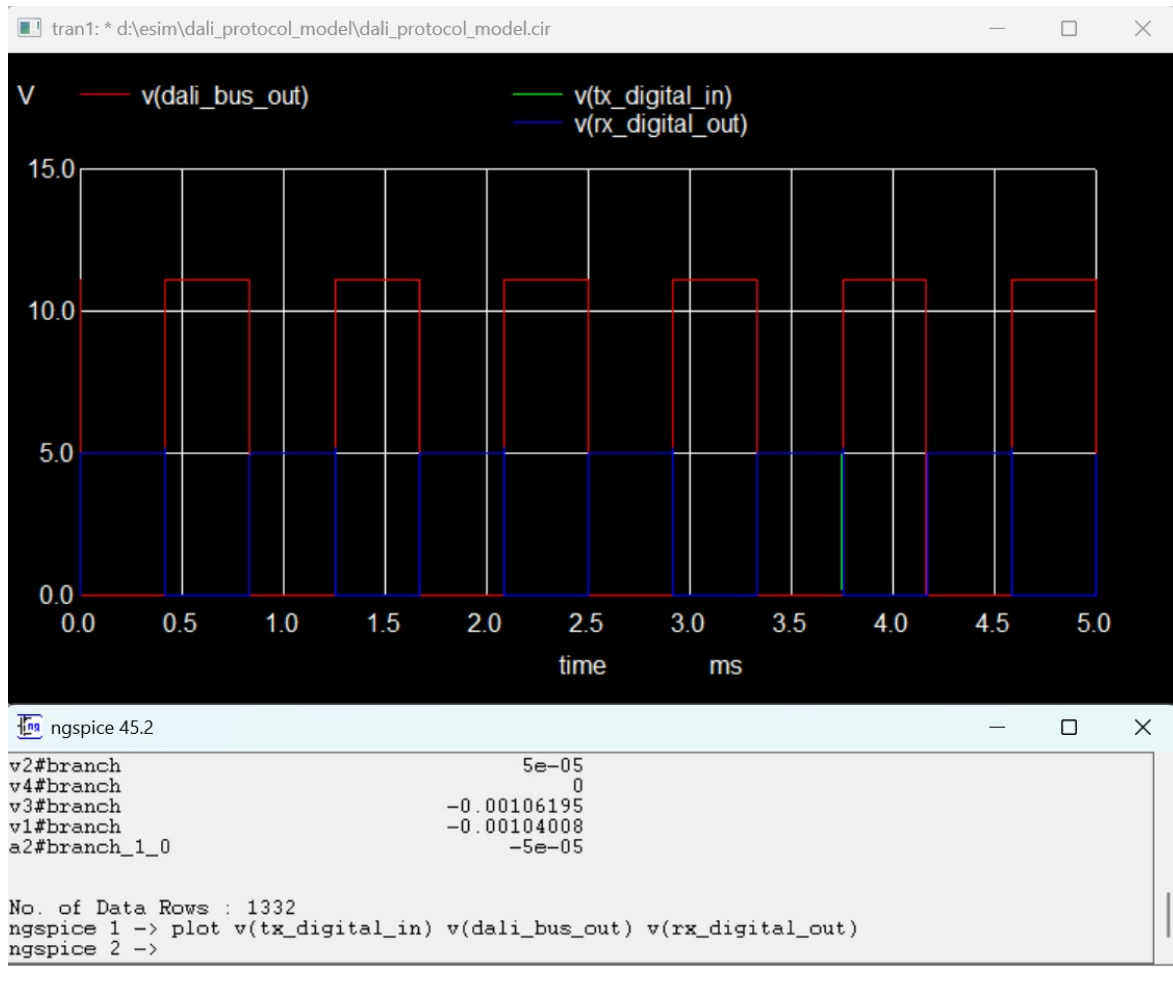


Figure 4: Tx_Digital_In (green) vs DALI_Bus_Out (red) — Manchester encoding verified

Figure 5 shows all three signals together — Tx_Digital_In (green), DALI_Bus_Out (red), and Rx_Digital_Out (blue). The end-to-end verification confirms that data is correctly encoded onto the DALI bus and successfully decoded at the receiver, with all bit transitions aligned.

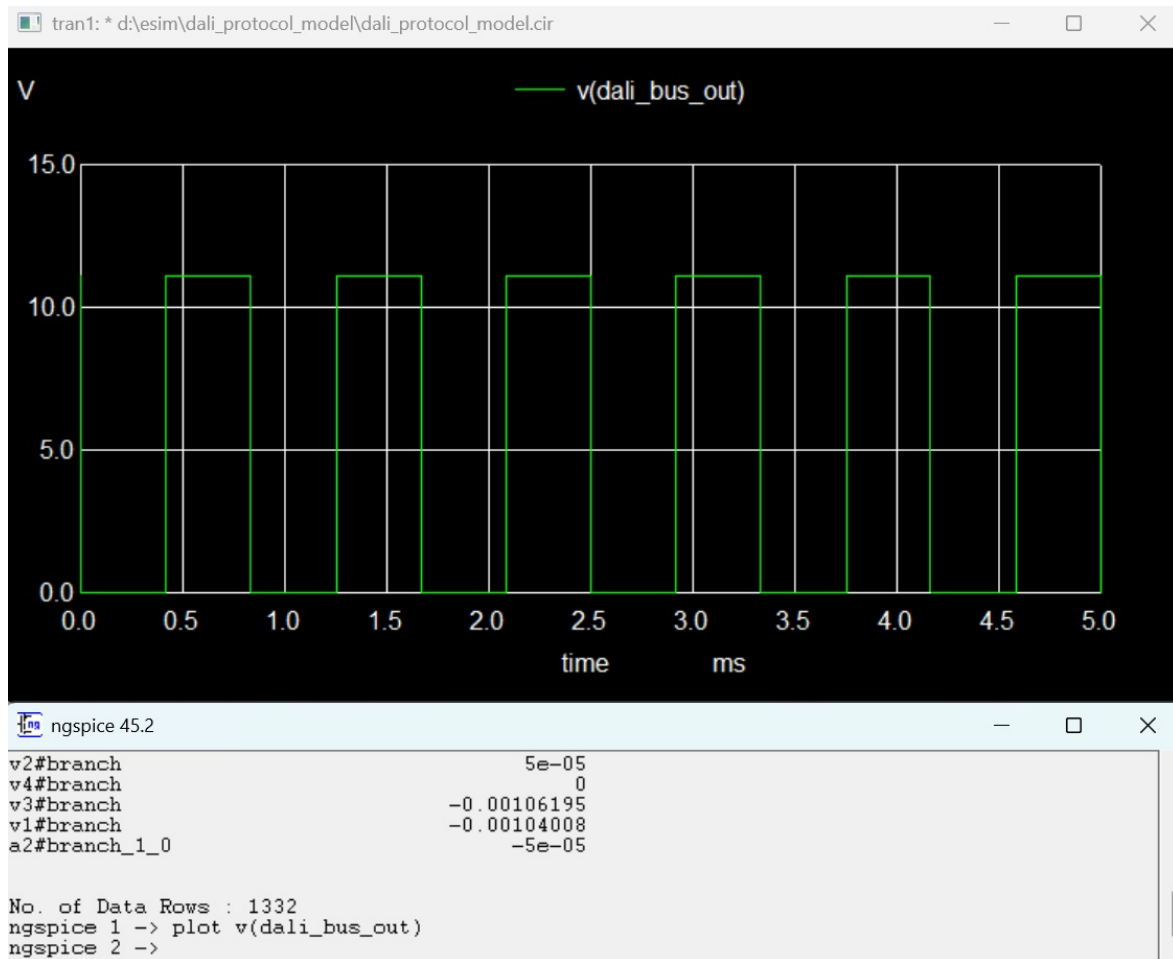


Figure 5: All signals — Tx_Digital_In, DALI_Bus_Out, Rx_Digital_Out (end-to-end)

Figure 6 shows the eSim Python plotting window with all nodes ticked. The yellow line (16V) is the DALI bus supply, red is DALI_Bus_Out, blue is Tx_Digital_In, and green is Rx_Digital_Out.

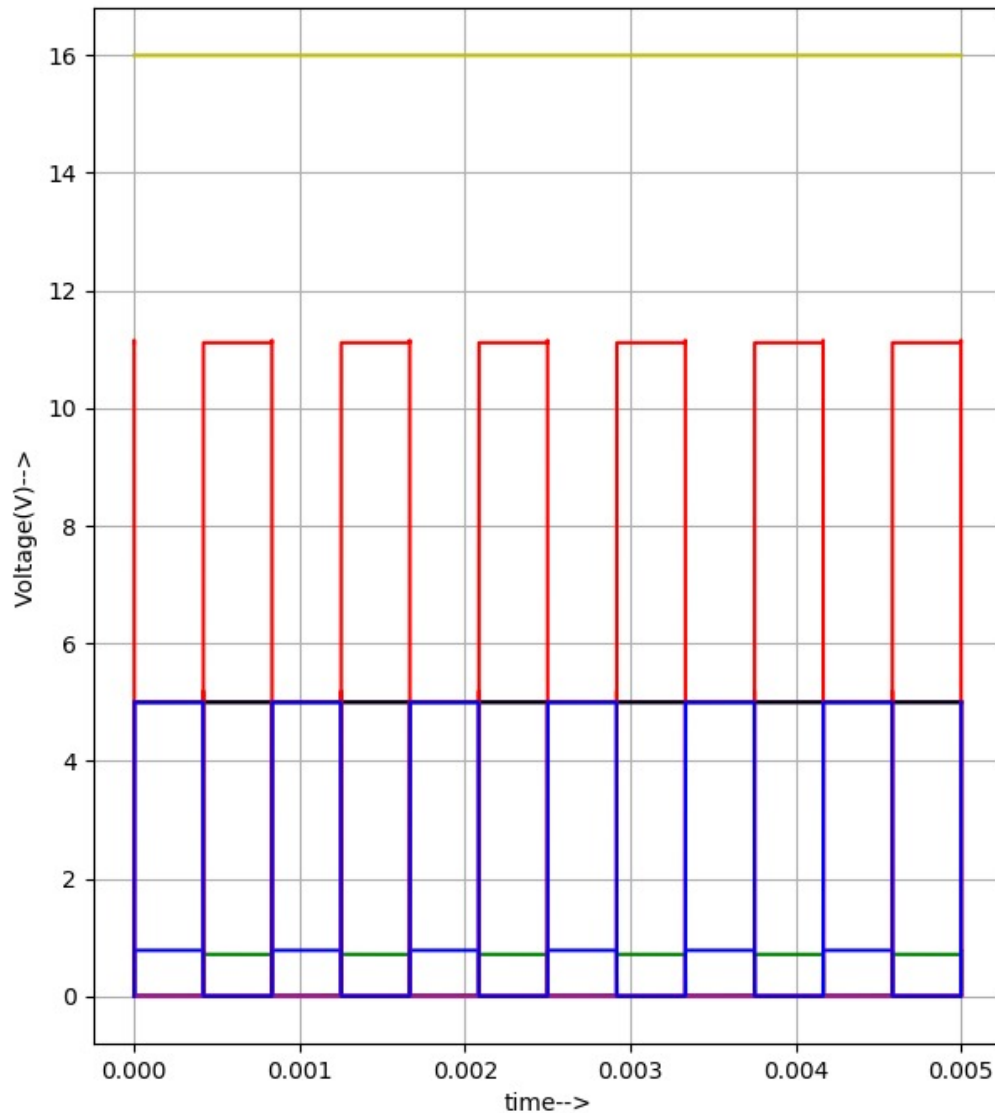


Figure 6: eSim transient analysis — all nodes plotted (supply 16V, DALI bus, TX input, RX output)

Results Summary

Stage	Node	Expected	Observed	Status
Digital input	Tx_Digital_In	0V/5V, 833us period	Clean square wave at 1200 bps	PASS
Manchester encoder	DALI_Bus_Out	Switching 0V to ~11V	Correct bus level switching	PASS
DALI LOW level	DALI_Bus_Out	Less than 9.5V	Pulled to 0V by transistor	PASS
DALI HIGH/idle	DALI_Bus_Out	Above 9.5V (16V)	Returns to ~11V when OFF	PASS
Manchester decoder	Rx_Digital_Out	Matches Tx pattern	Clean 0V/5V recovery	PASS
End-to-end	Tx vs Rx	Transitions aligned	All bit boundaries match	PASS

Conclusion

The DALI protocol transceiver simulation was successfully completed using eSim 2.1 and Ngspice 45.2. The transmitter produces correct Manchester encoded DALI bus waveforms with verified voltage levels. The receiver

correctly recovers the original digital bitstream. All six verification stages passed, confirming a functional DALI transceiver at 1200 bps per IEC 60929 and Microchip AN1465.

References

- [1] Husain, S. — DALI Communication, Microchip Technology AN1465, DS01465A, 2012
- [2] International Standard IEC 60929, Third edition 2006-01
- [3] International Standard IEC 62386-101, Edition 1.0 2009-06
- [4] eSim Documentation — fossee.in/esim | Ngspice User Manual — ngspice.sourceforge.net