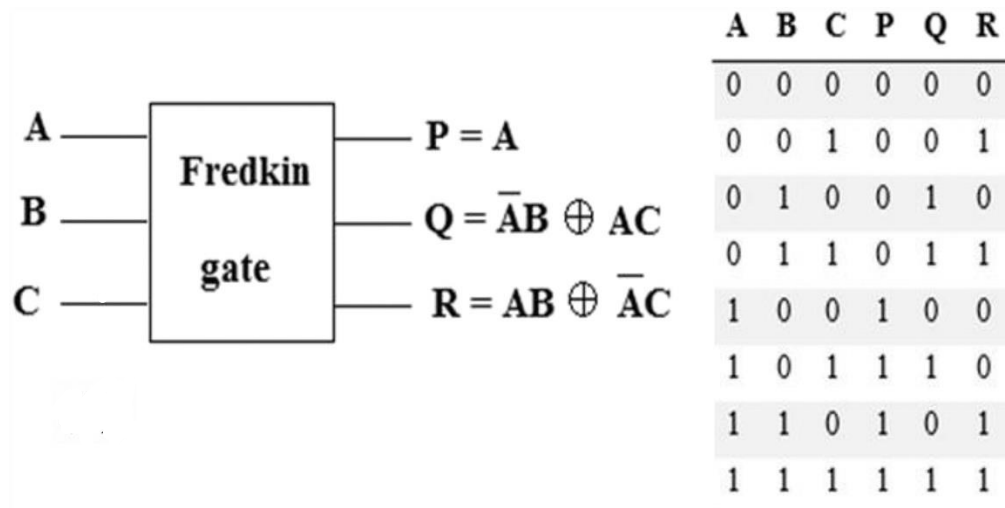


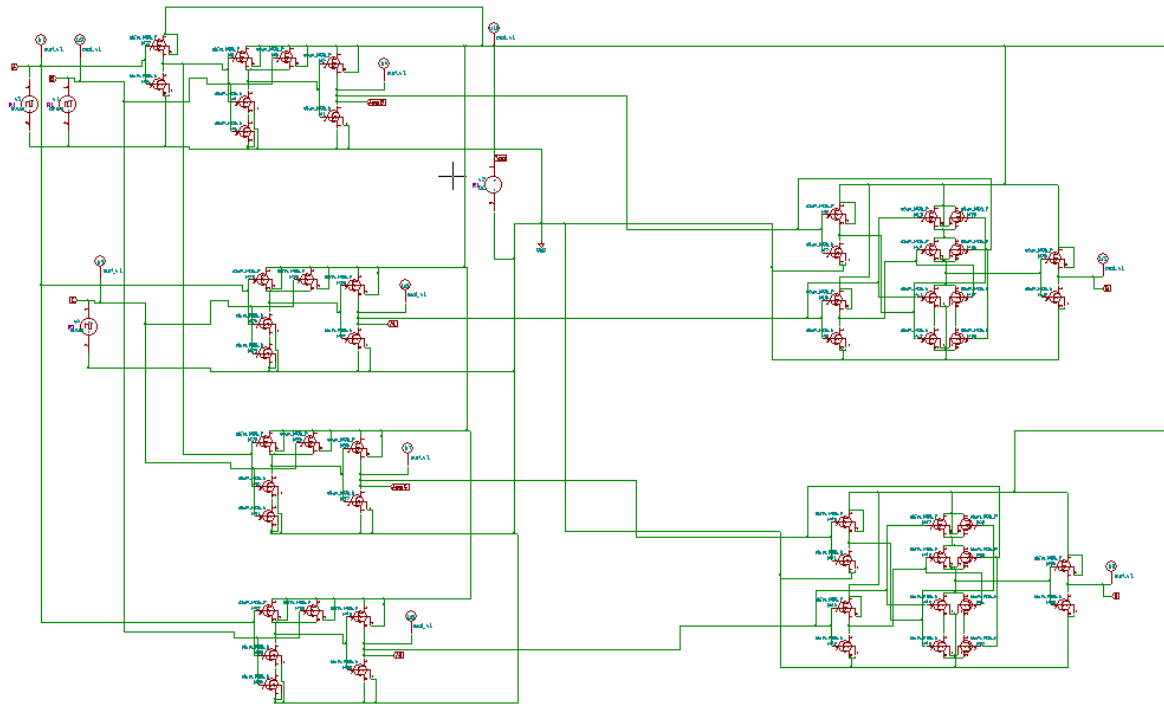
# Design Of Fredkin CSWAP Quantum Gate

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Abstract:

The Fredkin gate is named after physicist Edward Fredkin, who introduced the concept of reversible computing and contributed to the development of reversible logic gates. Reversible gates are important in quantum computing because they preserve information, making them useful for constructing quantum circuits where information must not be lost. Fredkin gate, also known as the Controlled SWAP (CSWAP) gate, is a three-bit reversible gate in quantum computing and reversible computing. It performs a controlled swap operation on three bits. The Fredkin gate swaps the second and third bits if the first bit (control bit) is set to 1 and leaves the bits unchanged if the control bit is 0. Reversible logic is also called information lossless logic, since the information embedded in the circuits can be recovered, if lost. A number of reversible gates were designed and invented. As examples like- the Fredkin gate, the Toffoli gate, the Peres gate, and the Feynman gate. Reversible logic has extensive applications and is considered as one of the futuristic technologies. But the logic circuit designing is based on logic gates, which are non-reversible. These logic gates help in future implementation of higher end circuits. In this paper an attempt is made to design logic gates using reversible gates and some of the higher end circuits are also designed such as Binary-to-Grey, grey-to-Binary, Adder, Subtractor etc.





CIRCUIT DIAGRAM OF FREDKIN GATE

Given Inputs:

- i) Transient analysis

Analysis
Source Details
Ngspice Model
Device Modeling
Subcircuits

Select Analysis Type

☐ AC
☐ DC
☒ TRANSIENT

Transient Analysis

Start Time

0

sec

Step Time

250

ms

Stop Time

24

sec

## ii) Source Details

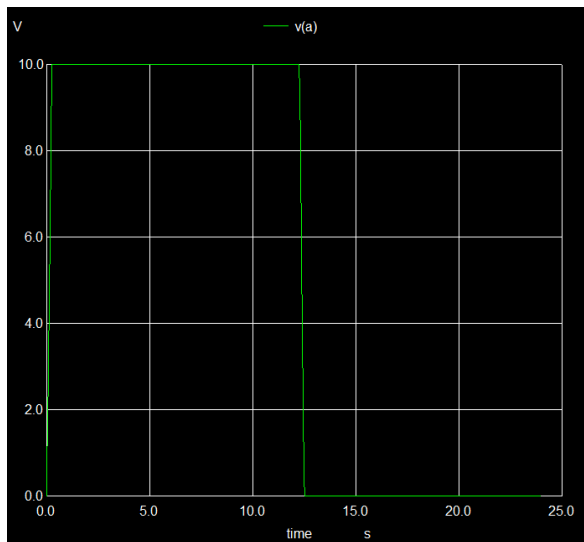
Analysis	Source Details	Ngspice Model	Device Modeling	Subcircuits
Add parameters for DC source v2				
Enter value (Volts/Amps):		10		
Add parameters for pulse source v3				
Enter initial value (Volts/Amps):		0		
Enter pulsed value (Volts/Amps):		10		
Enter delay time (seconds):		0		
Enter rise time (seconds):		0		
Enter fall time (seconds):		0		
Enter pulse width (seconds):		12s		
Enter period (seconds):		24s		
Add parameters for pulse source v1				
Enter initial value (Volts/Amps):		0		
Enter pulsed value (Volts/Amps):		10		
Enter delay time (seconds):		0		
Enter rise time (seconds):		0		
Enter fall time (seconds):		0		
Enter pulse width (seconds):		1s		
Enter period (seconds):		2s		
Add parameters for pulse source v4				
Enter initial value (Volts/Amps):		0		
Enter pulsed value (Volts/Amps):		10		
Enter delay time (seconds):		0		
Enter rise time (seconds):		0		
Enter fall time (seconds):		0		
Enter pulse width (seconds):		2s		
Enter period (seconds):		4s		

## iii) Mosfet Parameters-

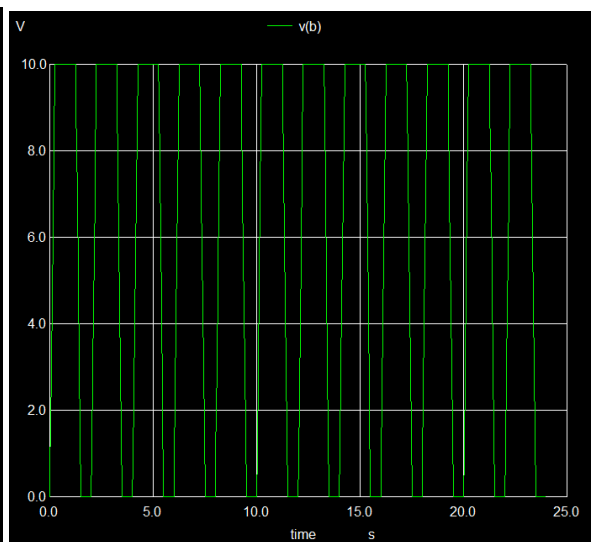
Add library for MOSFET m2 : esim_mos_p		delLibrary\MOS\PMOS-180nm.lib	Add
Enter width of MOSFET m2(default=100u):		0.9u	
Enter length of MOSFET m2(default=100u):		0.18u	
Enter multiplicative factor of MOSFET m2(default=1):		1	
Add library for MOSFET m1 : esim_mos_n		delLibrary\MOS\NMOS-180nm.lib	Add
Enter width of MOSFET m1(default=100u):		0.36u	
Enter length of MOSFET m1(default=100u):		0.18u	
Enter multiplicative factor of MOSFET m1(default=1):		1	

Verified Results (According to truth table):

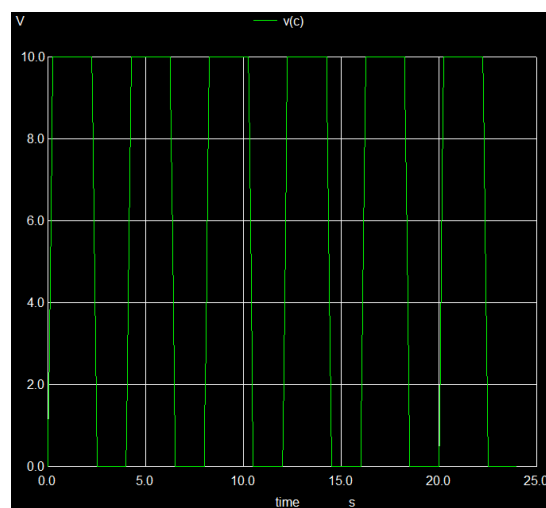
Inputs-



Output P=Input A

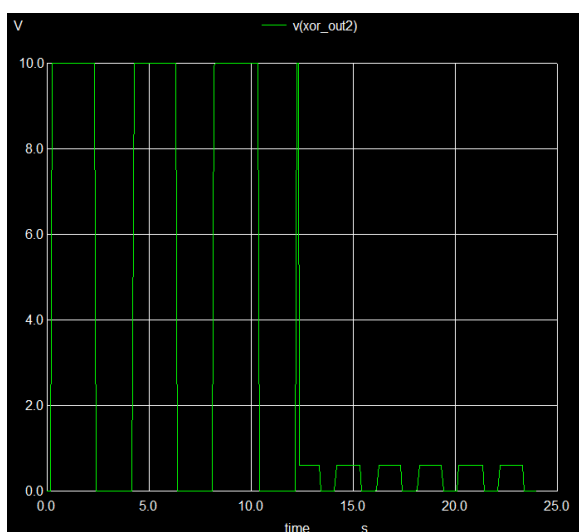


Input B

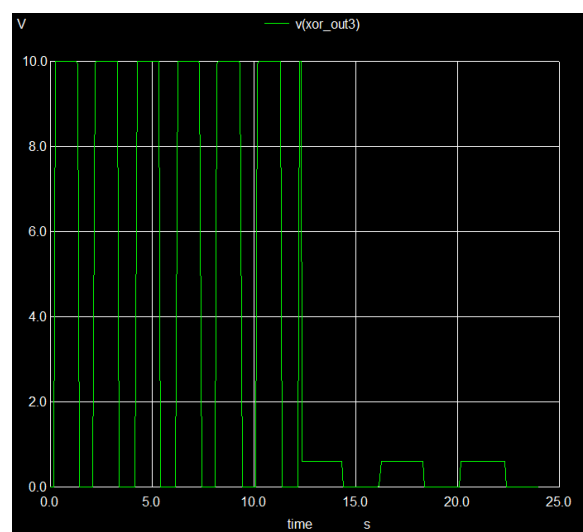


Input C

Outputs-



Output Q



Output R

#### Observation:

Thus from the given graphs we can observe that, whenever the input A is high the output bit Q and R are getting reversed else the output remains same as the input bits.

#### References:

<https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=9125070>

[https://en.wikipedia.org/wiki/Fredkin\\_gate](https://en.wikipedia.org/wiki/Fredkin_gate)

[https://www.researchgate.net/publication/320243483\\_A\\_Survey\\_on\\_Synchronous\\_and\\_Async\\_hronous\\_Counters\\_using\\_Reversible\\_Logic\\_Gates/figures?lo=1](https://www.researchgate.net/publication/320243483_A_Survey_on_Synchronous_and_Async_hronous_Counters_using_Reversible_Logic_Gates/figures?lo=1)