

Mod 8 Up/Down Synchronous Counter using 130nm CMOS Technology

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Abstract— In this study, 3 bit or mod 8 up/down synchronous counter is designed using transistors and Verilog code. This design is built with both analog and digital circuitry. As the counter is synchronous, the clock signal is applied to all of the flipflops at the same time. Here, an astable multivibrator is used to generate the clock signal. The analog circuitry consists of the astable multivibrator, the combination of AND gates and XOR gate implemented using CMOS transistors. The digital circuitry of MOD - 8 is made up of three T flipflops with synchronous clear. The control input M=0 is assumed for UP counting and M=1 for DOWN counting. The entire design process of sequential circuits and simulations are carried out using eSim software.

Keywords— Synchronous counter, T flipflop, CMOS, Astable multivibrator

[1] Reference Circuit Details and Waveforms

In 3 bit or mod-8 Up or Down counting, 3 Flip Flops are required, which can count up to $2^3-1 = 7$. Here, the counter's mode control input determines which sequence will be generated. In this scenario, the counter's mode control input determines whether it will execute up counting or down counting. Such a counter must be designed similarly to a synchronous counter, but it also needs additional combinational logic for mode control input.

Here 3 T flipflops are designed using Verilog code. For the control input (M), let's assume M=0 for UP counting and M=1 for DOWN counting.

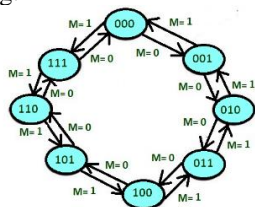


Fig.1: State transition diagram of 3 bit up/down counting

For the generation of clock pulse, the astable multivibrator is constructed by cascading three inverters, and the clock pulse signal is produced using a resistor and capacitor. The inverters serve as a buffer, and an important factor in switching the inputs and outputs of the inverter is the direction in which the capacitor is charged and discharged.

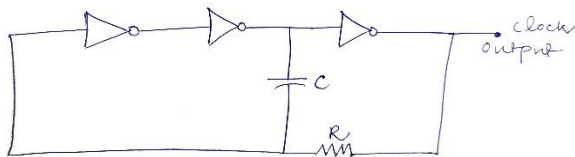


Fig.2: Block diagram of astable multivibrator

When the clock pulse is applied and input T of the flip-flops, the present states of the counting sequence, as well as the next states are represented by the circuit excitation table. Using the Flip Flops excitation table, we can determine the input values for 3 Flip Flops by observing the change from one state to the subsequent state. In table 1, the excitation table is created using the necessary counting sequence.

Further, the circuit excitation table is reduced using the K-map to obtain the Boolean functions for the input to the flipflops. To create circuit schematics, the simplified expression for Flip Flops is adopted. In this case, all connections are formed using reduced expressions for flip flops shown in fig.3.

The Boolean functions for input of flipflops are, For

$$T_3 = M'Q_2Q_1 + MQ_2'Q_1'$$

$$T_2 = M'Q_1 + MQ_1'$$

$$T_1 = 1$$

In analog part of this counter, an astable multivibrator, combinational logic of flipflop inputs and control input (M) are designed using CMOS transistors.

	Control Input (M)	Present State			Next State			Flipflop Inputs		
		Q ₃	Q ₂	Q ₁	Q ₃	Q ₂	Q ₁	T ₃	T ₂	T ₁
UP Counting	0	0	0	0	0	0	1	0	0	1
	0	0	0	1	0	1	0	0	1	1
	0	0	1	0	0	1	1	0	0	1
	0	0	1	1	1	0	0	1	1	1
	0	1	0	0	1	0	1	0	0	1
	0	1	0	1	1	1	0	0	1	1
	0	1	1	0	0	0	1	0	0	1
	0	1	1	1	0	1	1	0	0	1
DOWN Counting	1	0	0	0	1	1	0	1	1	1
	1	0	0	1	0	0	0	0	0	1
	1	0	1	0	0	0	1	0	1	1
	1	0	1	1	0	1	0	0	0	1
	1	1	0	0	0	0	1	1	1	1
	1	1	0	1	1	0	0	0	0	1
	1	1	1	0	1	1	0	0	1	1
	1	1	1	1	1	0	1	0	0	1

Table.1: Circuit excitation table for 3 bit up/down counting

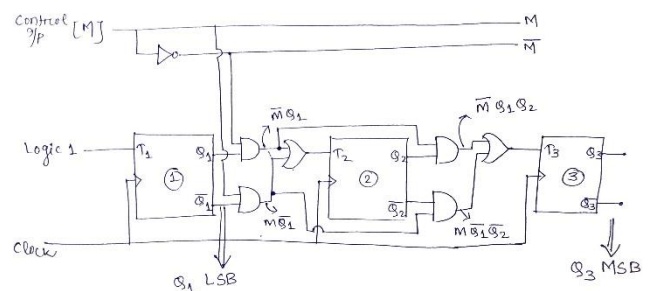


Fig.3: Block diagram of mod 8 up/down synchronous counter

Here, a clock pulse with a +ve edge trigger is used as a toggle.

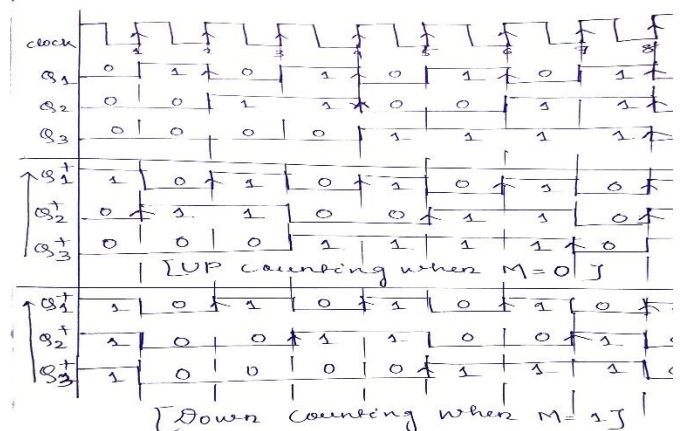


Fig.4: Timing diagram of 3-bit up/down synchronous counter

References

- [1] https://www.researchgate.net/publication/312195862_Rapid_low_power_Synchronous_circuits_using_transmission_gates