

Design and Implementation of frequency divider mixed signal circuit performed in eSim

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Abstract— An electrical circuit known as a frequency divider splits a given frequency by an integer value of n . The input frequency is divided by four using a divide-by-4 circuit in this instance. An astable multivibrator and a divide-by-4 counter make up the two components that make up the frequency divider. RF devices, communication, frequency synthesizers, and other audio-based systems all depend on frequency dividers.

A divide-by-4 counter and an astable multivibrator make up the Frequency Divider. A clock signal with a particular frequency is generated by the astable multivibrator and used as an input by the counter. The counter then generates an output signal with a frequency that is divided. In this, all processes have been carried out of a CMOS-based frequency divider using Open-Source Software eSim, etc.

Keyword—eSim tool,

I. INTRODUCTION

The bit rates used by serial data transmission systems today range from 10 to 40 Gb/s. Most modern communication integrated circuits (ICs) use GaAs, InP, or SiGe bipolar technology. There have been some high-speed CMOS chips disclosed, confirming that CMOS is a good solution for designing broadband circuits since cutting-edge circuit approaches and cutting-edge fabrication processes can be combined to increase speed limitations. The lower production costs, higher yield, and integrated density make this strategy very cost-effective.

frequency divider in IBM 130nm CMOS is presented. The manufactured nMOS transistors have a f_t of 100 GHz. All subcircuits of this frequency divider use current-mode logic (CML) with differential signals

REFERENCE CIRCUIT DETAILS

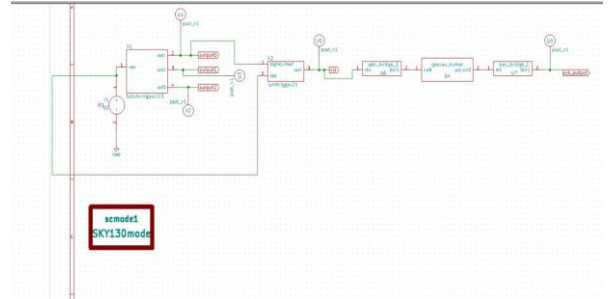
Astable Multivibrator

A free-running multivibrator is another name for the astable multivibrator. It possesses two quasi-stable states, and state shifts can be produced without the use of an outside stimulus. The length of time that each state of the circuit will last is determined by the component values. Typically, an astable multivibrator is employed to create a square wave as it alternates between two states. The resistance and capacitor values in this circuit determine the time period. Additionally, it is influenced by the op-upper amps and lower threshold voltages

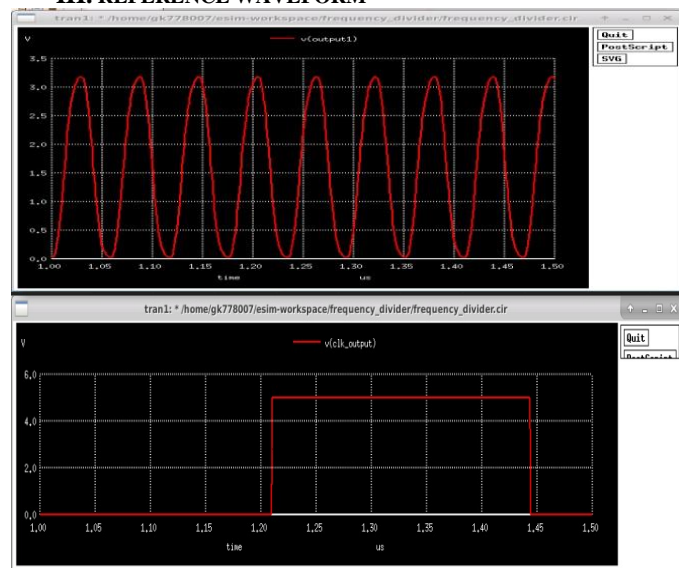
MOD-4 Counter

A binary divider with an inverted output terminal that is connected back to the data terminal in a feedback loop is known as a Divide-By-4 counter. It is made up of two D flip flops. It is an asynchronous counter where each subsequent flip-flop is clocked by the output of the flip-flop before it, with the initial flip-flop being clocked by the external clock pulse. It takes some time at each stage as the signal moves in a ripple pattern, resulting in the lower frequency at the output.

II. REFERENCE CIRCUIT DESIGN



III. REFERENCE WAVEFORM



IV. REFERENCE PAPER

- https://github.com/PatelVatsalB21/Mixed_Signal_Frequency_Divider
- <https://www.bing.com/search?q=frequency+divider+using+cmos&qsn=&form=QBRE&sp=1&pq=frequency+divider+using+cmos&sc=9-28&sk=&cvid=C83C9014852142D7AF7944D39E98E2A9&ghsh=0&ghacc=0&ghpl=>