

D Flip-Flop based SRAM cell using CMOS technology

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Abstract:

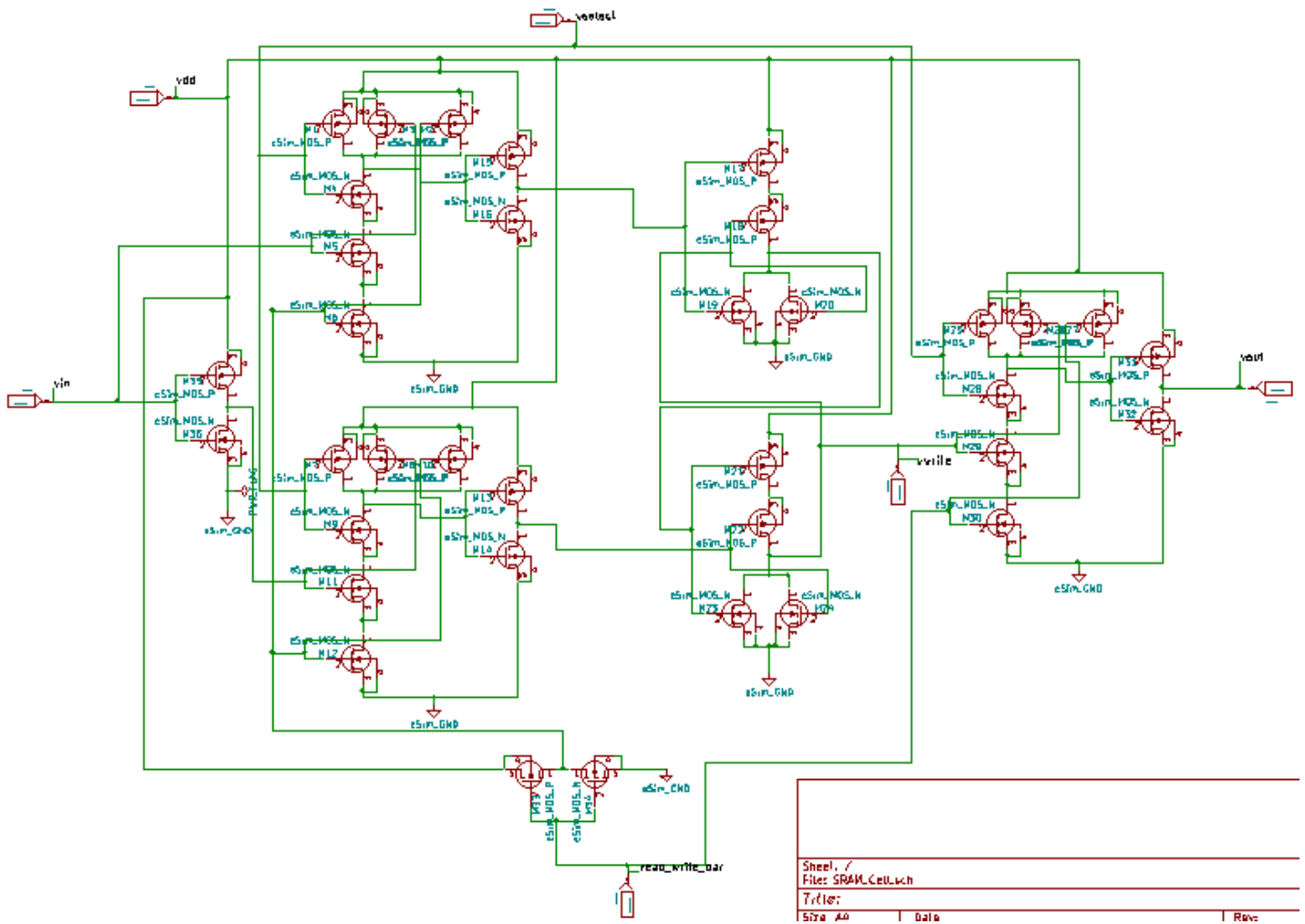
Nowadays data is the fuel for every industry as well as our society. To store any kind of data memory plays an important role. Here I have worked upon the design of D flip-flop based Static Random Access Memory (SRAM) cell with the CMOS technology using eSim, Ng Spice and Sky130 nm PDK. It is used to design cache memory. It is capable of holding data as long as power is supplied. The number of chips in SRAM is more than the other RAM variants which makes it costly. However, the performance of SRAM is very expeditious. The power consumption is less as it does not need of refresh cycle over the period. Due to lower density, it can be implemented where the lower amount of memory is required. For designing L1 and L2 cache memory SRAM is well suited.

Circuit Details:

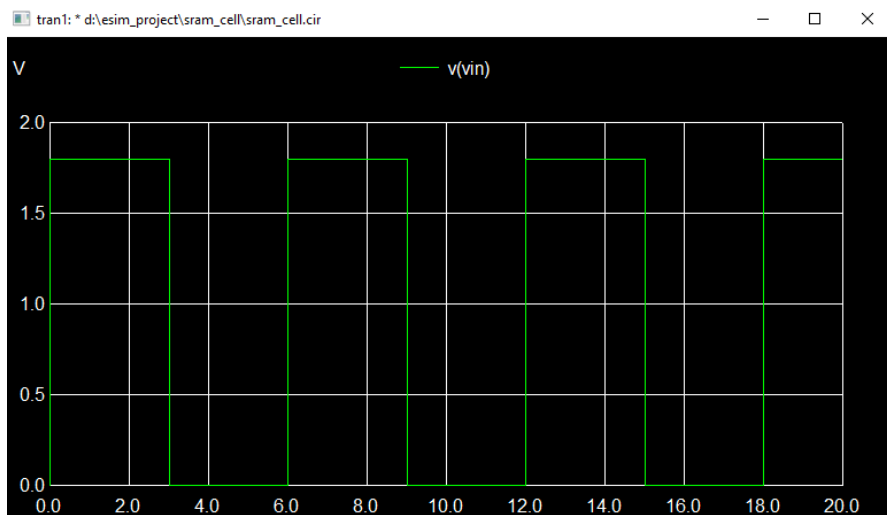
Random Access Memory is also known as volatile memory. Regardless of the technology, all RAM memory cells must have the four functions: Data-input, Data-output, select line and Read or Write bar. For making an SRAM cell, here we used three numbers of 3-input AND gate, two numbers of 2-input NOR gate and two numbers of NOT gate. All the logic gates are designed with Complementary Metal Oxide Semiconductor or CMOS inverter circuit as the CMOS consumes less power to work and has higher switching speed. We have designed a single cell of D flip-flop based Static RAM or SRAM using 130 nm technology on eSim circuit simulation software. This design of SRAM works functionally correct but it is not more practically used.

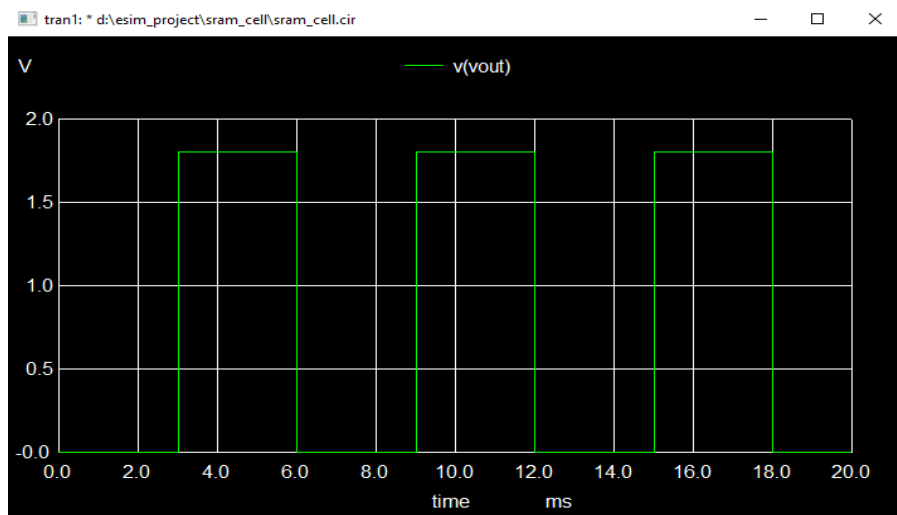
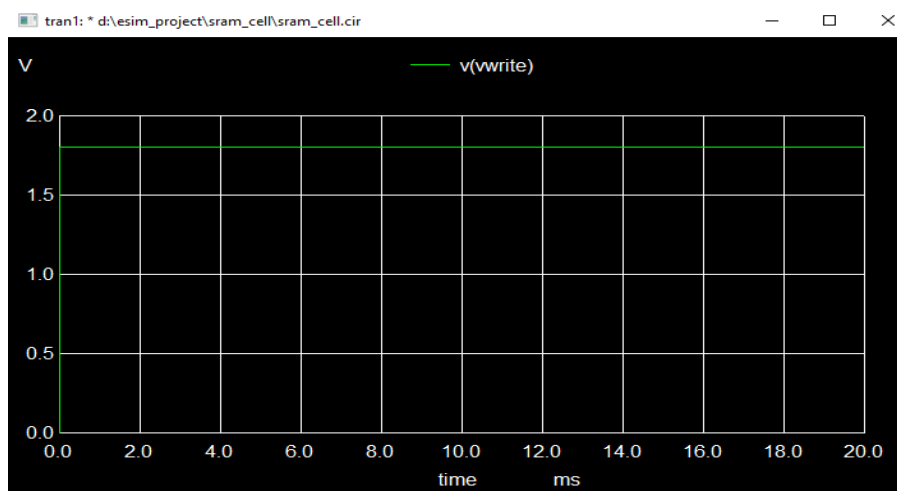
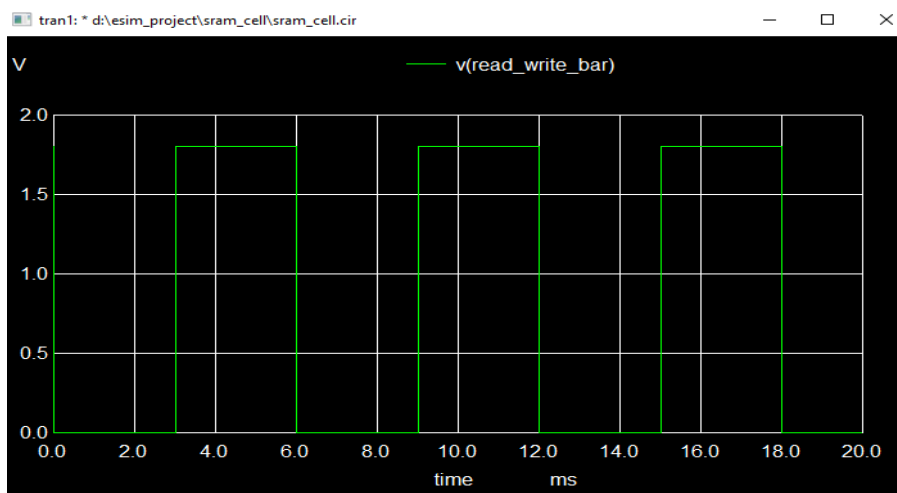
It works in a simple but interesting way. The Read/Write-bar data controls the working of the whole RAM. When Write-bar will be activated (logic 0) the input data will be stored in RAM. To get the stored data at output the Read input logic must be high. This output data will be immutable until the Write-bar logic will be 0 means active in the next time.

Schematic Diagram:



Implemented Waveforms:





References:

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- [4] S. A. Madhu Shaky. Design low power CMOS D flip flop using modified svl techniques. <https://www.ijrar.org/papers/IJRAR1944229.pdf>