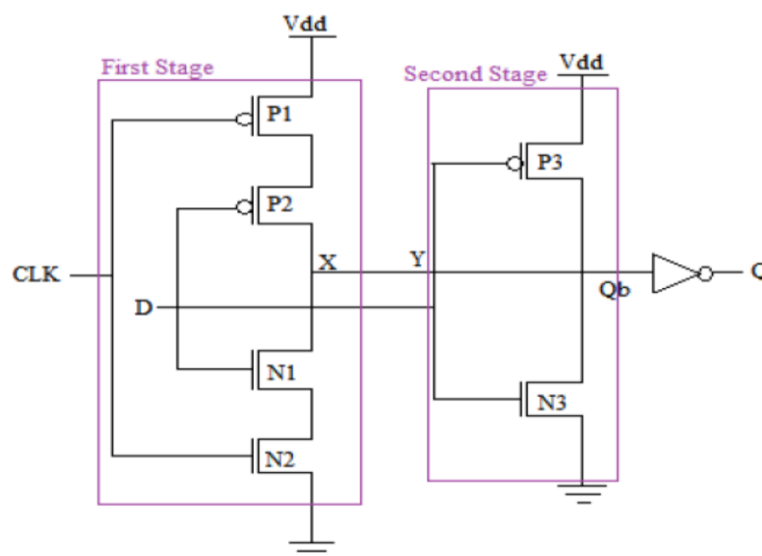
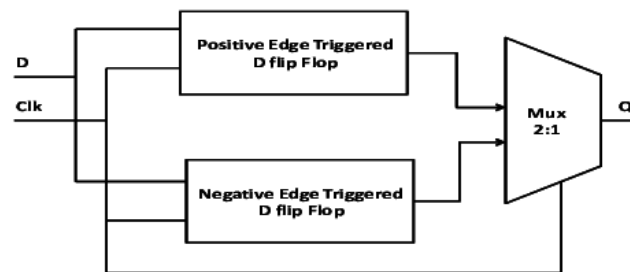


Double-edge-triggered D-flip-flops for high-speed CMOS circuits

Project Description

A Double-Edge-Triggered D Flip-Flop (DET-DFF) is a sequential logic element that captures input data on both rising and falling edges of the clock signal, unlike conventional single-edge flip-flops that only trigger on one edge. This makes DET-DFFs highly attractive for high-speed CMOS circuits, where power and performance are critical.

By sampling data on both edges, DET-DFFs effectively double the data throughput without increasing the clock frequency. This reduces clock distribution power, clock skew issues, and electromagnetic interference, making them well-suited for low-power, high-performance VLSI systems, such as microprocessors, digital signal processors, and communication ICs.



Expected Outcomes

1. A **functional DET-DFF circuit** implemented in CMOS.
2. **Comparison of performance metrics** (power, delay, PDP) with conventional DFFs.
3. Demonstration of **high-speed and low-power advantages** for VLSI applications.

Output

Two circuits are proposed for double edge-triggered D flip-flops (DETDFs). A DETDFF responds to both edges of the clock pulse. As compared with positive or negative edge-triggered flip-flops, a DETDFF has advantages in terms of power dissipation and speed. Delay figures for these circuits are measured by simulation. It is shown that these circuits are faster and have lower transistor counts than previously reported circuits. It is shown that these flip-flops can be used at 320-400-MHz clock frequency