DESIGN AND SIMULATION OF A TWO-STAGE MILLER-COMPENSATED CMOS OPERATIONAL AMPLIFIER

Circuit Simulation Project

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Abstract

This project presents the design and simulation of a two-stage Miller-compensated CMOS operational amplifier using the open-source eSim/ngspice simulation environment. The amplifier consists of an NMOS differential input stage with a PMOS current-mirror active load, followed by a second common-source gain stage. A biasing network is used to establish the required operating current, while a Miller compensation capacitor with a series nulling resistor is used to improve the frequency response and stability of the amplifier.

The circuit is simulated with a supply voltage of 1.8 V, a common-mode voltage of 0.9 V, and a bias current of 10 μA. AC analysis is performed from 1 Hz to 100 MHz using a logarithmic frequency sweep. The simulated open-loop gain is approximately 61 dB at low frequency, and the gain crosses 0 dB in the tens-of-megahertz range. The frequency response shows the expected dominant-pole roll-off, while the phase response varies smoothly with frequency.

1 Theory

A CMOS operational amplifier is a high-gain differential amplifier used as a basic building block in analog integrated circuits. A two-stage topology is commonly used when high voltage gain is required.

The first stage of the proposed amplifier is an NMOS differential pair with a PMOS current-mirror active load. The differential pair converts the difference between the input voltages into a differential current. The active load provides high output resistance and converts the differential signal into a single-ended signal.

The second stage is a common-source gain stage that provides additional voltage gain and drives the output node.

A major issue in a two-stage amplifier is the presence of multiple high-frequency poles. These poles can introduce excessive phase shift and may cause instability when the amplifier is used in a feedback configuration.

Miller compensation is used to overcome this problem. A compensation capacitor is connected between the first-stage output and the final output node. Due to the Miller effect, the effective capacitance at the first-stage output is increased, resulting in pole splitting. This creates a dominant pole at a lower frequency and pushes the non-dominant pole toward a higher frequency.

A resistor is connected in series with the Miller capacitor. This nulling resistor modifies the feed-forward path created by the compensation capacitor and helps control the associated zero.

2 Circuit Description

The implemented circuit consists of the following main sections:

- NMOS differential input pair.
- PMOS current-mirror active load.
- NMOS bias/current-source transistors.
- Second common-source gain stage.
- Miller compensation network.
- Capacitive output load.

The differential input stage consists of MN1 and MN2. Their sources are connected to the bias current network, while their drains are connected to the PMOS active-load network.

MP3 and MP4 form the PMOS current-mirror active load. This arrangement provides high output resistance and converts the differential current into a single-ended signal.

The second gain stage consists primarily of MP6 and MN7. This stage provides additional voltage gain and produces the final output.

MN5 and MN8 are used in the biasing network. The bias current used in the simulation is $10\,\mu$A.

The main supply and input conditions are

$$V_{DD} = 1.8\,\text{V} \tag{1}$$

$$V_{CM} = 0.9\,\text{V} \tag{2}$$

and

$$I_{bias} = 10\,\mu\text{A}. \tag{3}$$

The Miller compensation network uses

$$C_C = 0.8\,\text{pF} \tag{4}$$

with a series resistor of

$$R_Z = 2.2\,\text{k}\Omega. \tag{5}$$

The output load capacitance is

$$C_L = 1\,\text{pF}. \tag{6}$$

The MOS devices are simulated using the eSim model libraries `NMOS-0.5um.lib` and `PMOS-0.5um.lib`. The transistor configurations shown in the simulation use a channel length of approximately $0.85\,\mu$m.

3 Circuit Schematic

Figure 1 shows the implemented two-stage Miller-compensated CMOS operational amplifier in eSim.

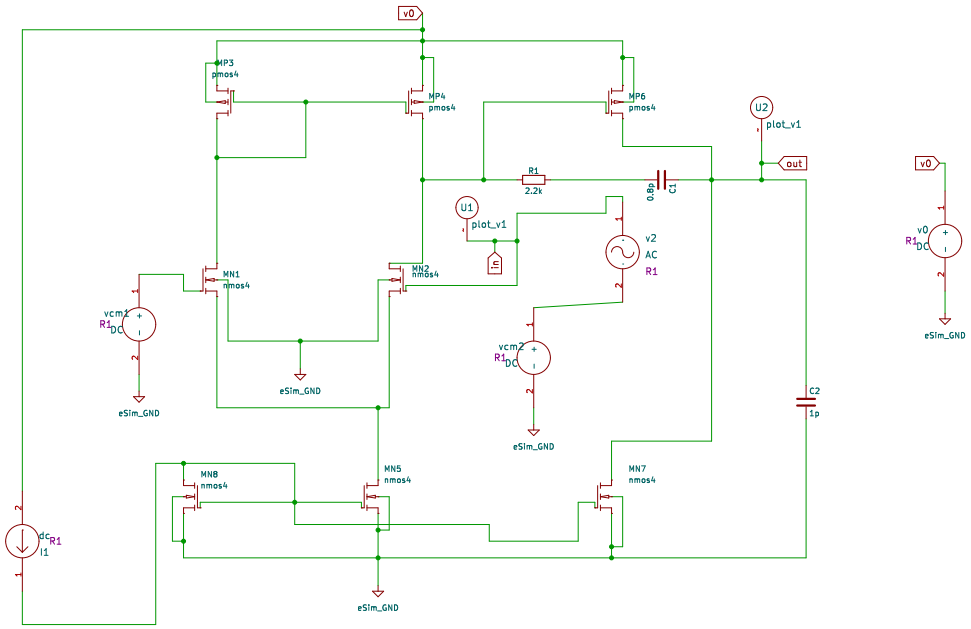

Figure 1: Two-stage Miller-compensated CMOS operational amplifier schematic implemented in eSim

4 Simulation Results

The AC analysis is performed from 1 Hz to 100 MHz using a decade sweep with 100 points per decade. The AC input amplitude is set to 1 V with zero phase.

4.1 Magnitude Response

The simulated open-loop magnitude response is shown in Figure 2.

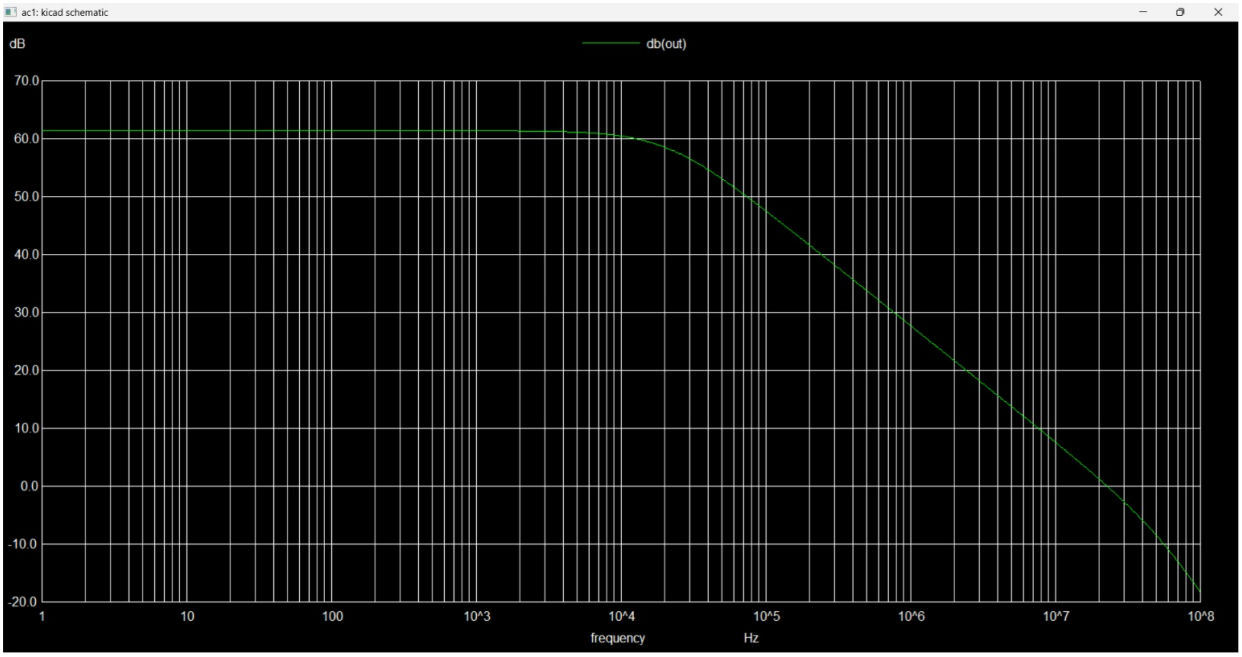

Figure 2: Simulated open-loop magnitude response.

The low-frequency gain is approximately 61 dB. The response remains nearly constant at low frequencies and then decreases with an approximately -20 dB/decade slope after the dominant pole.

The gain reaches approximately 0 dB in the tens-of-megahertz range, giving a unity-gain bandwidth of approximately 20–23 MHz from the plotted response.

4.2 Phase Response

The simulated phase response is shown in Figure 3.

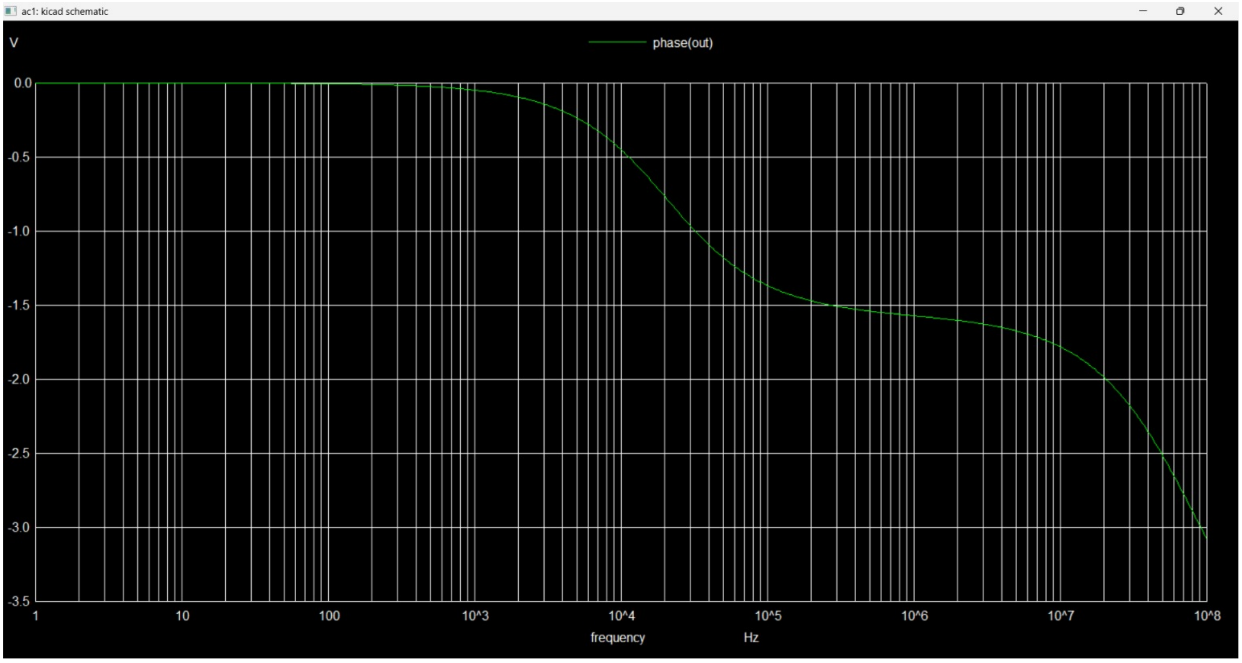

Figure 3: Simulated phase response of the amplifier.

The phase remains close to zero at low frequencies and decreases as the frequency increases. The response shows a smooth phase variation, which is consistent with the intended effect of the Miller

compensation network and the series nulling resistor.

5 Conclusion

A two-stage Miller-compensated CMOS operational amplifier was successfully designed and simulated using the open-source eSim/ngspice environment. The proposed circuit consists of an NMOS differential input stage with a PMOS current-mirror active load, followed by a second common-source gain stage and a biasing network.

The simulated amplifier achieved a **low-frequency open-loop gain of approximately** 61 dB. The magnitude response showed a controlled roll-off of approximately -20 dB/decade after the dominant-pole region. The **unity-gain frequency was approximately** 23 MHz, demonstrating useful bandwidth for the designed two-stage amplifier.

The phase response also demonstrated good frequency compensation. At the unity-gain frequency, the simulated phase was approximately $-116°$, resulting in a **phase margin of approximately** $63°$. This indicates that the amplifier has a reasonable stability margin and that the Miller compensation network effectively controls the high-frequency behavior.

The 0.8 pF Miller compensation capacitor provides pole splitting, while the 2.2 kΩ series nulling resistor helps control the compensation zero. Overall, the design achieves a good balance between gain, bandwidth, and stability.

Key Simulation Results
DC Gain: 61 dB **Unity-Gain Frequency:** 23 MHz
Phase Margin: $\approx 63°$

These results demonstrate the effectiveness of the proposed Miller-compensated two-stage CMOS operational amplifier and its suitability for transistor-level analog circuit design and analysis using eSim/ngspice.

References

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2. B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, 2001.
3. P. Vimala, C. G. Gokhale, R. Dhirendra Rao, and Aneesh V. S., "Design of Two Stage Miller Compensated CMOS Opamp with Nulling Resistor in 90nm Technology," IEEE, Document 10527553.
4. FOSSEE, Indian Institute of Technology Bombay, *eSim – Open Source EDA Tool*.