Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

The Circuit Simulation Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for designing and simulating electrical and electronic circuits for learning and application purposes. The objective is to create and document original, application-based, or proof-of-concept circuit designs using eSim to build an open-source resource database.

Name of the participant : Madhvesh Kapadia

Affiliation / Institution : School of Electronics and Electrical Engineering, VIT Bhopal University, Sehore, Madhya Pradesh, India.

Title of the circuit: Design and simulate Transistor-based PS/2 Interface in eSim.

Theory:

The PS/2 communication standard is a synchronous serial protocol operating at $+5V$ logic using an open-collector bus architecture. In this design, the physical layer transceiver is implemented using discrete NPN transistors in eSim instead odf dedicated ICs or microcontrollers. The circuit consists of three core functional stages:

1. Autonomous Clock Generator: A symmetric cross-coupled BJT astable multivibrator(Q_1, Q_2) generates the continuous protocol clock (PS2_CLK). With $R_B = 56k\Omega$ and $C = 1\ nF$, the clock frequency is

$$f_{clk} = \frac{1}{2 \cdot ln(2) \cdot R_B \cdot C} \approx 12.88\ kHz$$

which satisfies the standard 10.0 kHz to 16.7 kHz specification.

2. Transmitter Open-Collector Stage: An open-colletor NPN switching transistor (Q_3) drives the serial data bus (PS2_DATA). A $4.7\ k\Omega$ pull-up resistor (R_6) and a $200\ pF$ capacitor (C_3) model transmission cable loading and exponential rise-time dynamics ,i.e,

$$t_r \approx 2.2 \cdot RC \approx 2.07\ \mu s$$

which is is well within the protocol maximum limit $t_r \leq 5.0\ \mu s$.

3. Receiver Signal Restoration: Dual-stage cascaded Resistor-Transistor Logic (RTL) inverters (Q_4 – Q_5 for clock and Q_6 – Q_7 for data) act as active non-inverting buffers. They eliminate capacitive edge rounding and regenerate clean rail-to-rail 0 to %V digital logic levels (RX_CLK_OUT and RX_DATA_OUT).

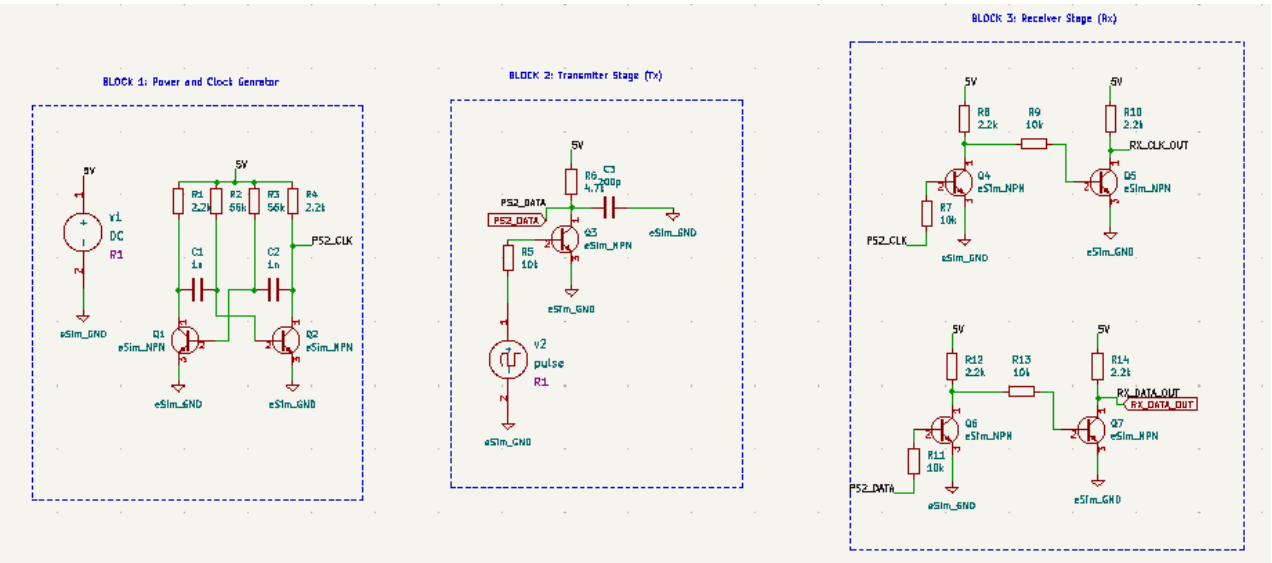
Reason to simulate with eSim :

eSim integrates KiCad schematic capture with the Ngspice simulation engine, providing an open-source platform to analyze transistor switching dynamics. Simulating this circuit in eSim enables verification of non-linear BJT saturation, multivibrator startup transients with initial contion (.ic) and transmission line capacitive loading delays without relying on the proprietary SPICE tools. It serves as a prrof-of-concept for understanding physical-layer line driving and discrete digital signal restoration.

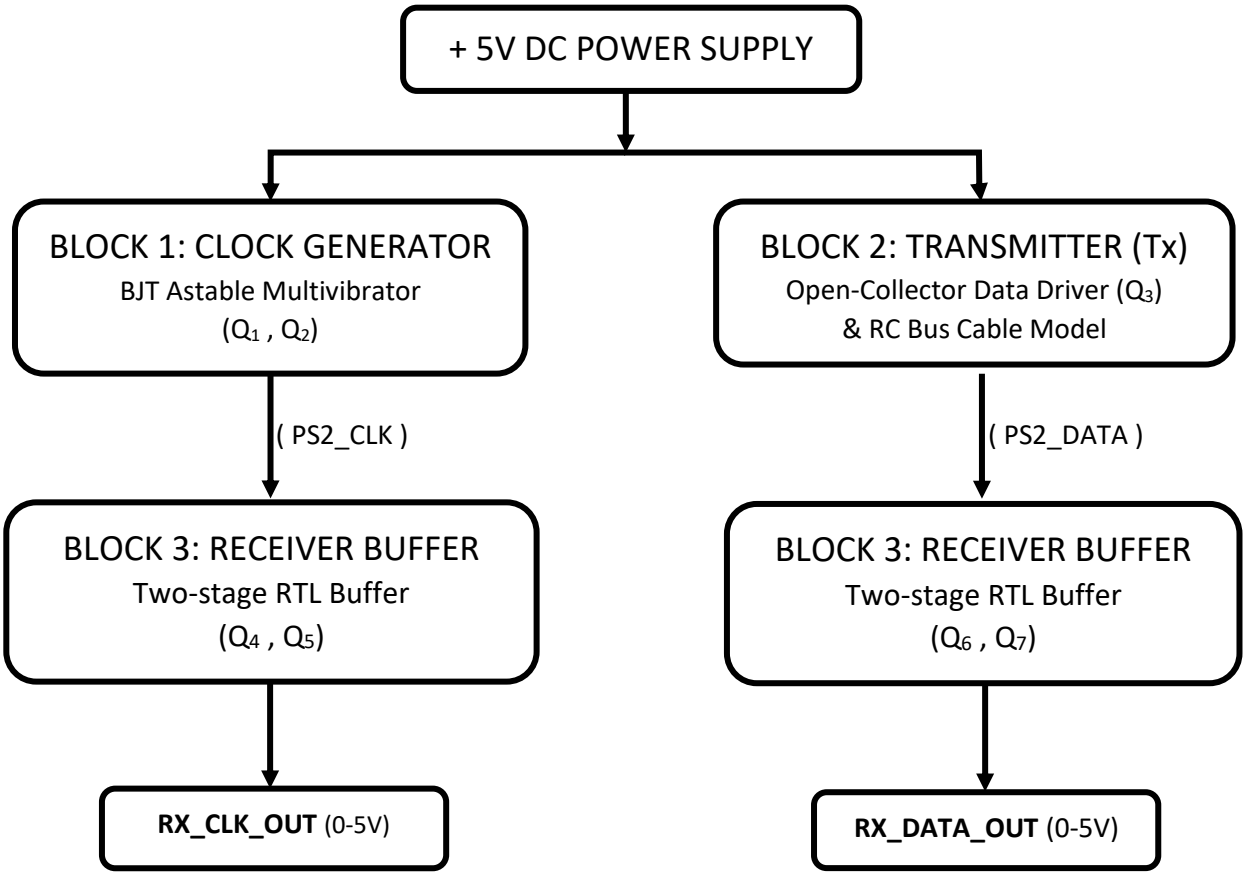
Expected Outcome/outputs :

- Continuous square-wave generation on PS_CLK at $\sim 12.88\ kHz$ with a $\sim 50\%$ duty cycle.
- Open-collector switching on PS2_DATA with exponential rise time, $t_r \approx 2.07 \mu s$, compliant with the standard PS/2 timing window.
- Clean signal reconstruction at the receiver stage, outputting restored 0 to 5V digital waveforms on RX_CLK_OUT and RX_DATA_OUT with transition times under 200 ns.

Circuit Diagram(s) :



Block Diagram (s) :



Expected Results :

- **DC Supply Voltage (v_1):** 5V.
- **PS2_CLK Line:** Square wave oscillating between $0.18V$ and $5.0V$ at $\sim 12.88\ kHz$.
- **PS2_DATA Line:** Modulated serial pulse levels between $0.18V$ and $5.0V$ with exponential RC rise time $t_r \approx 2.07\mu s$.
- **RX_CLK_OUT:** Restored: to 5V square wave in-phase with the clock source.
- **RX_DATA_OUT:** Restored 0 to 5V non-inverted serial data bitstream with sharp edges.

Source/Reference(s):

- Wikipedia, “Multivibrator”: https://en.wikipedia.org/wiki/Multivibrator.
- University of Toronto ECE, “The PS/2 Mouse/Keyboard Protocol”: https://www-ug.eecg.utoronto.ca/desl/nios_devices_SoC/datasheets/PS2%20Protocol.htm.
- Wikipedia, “PS/2 Port”: https://en.wikipedia.org/wiki/PS/2_port.