Circuit-Level Modelling and Verification of an SDI-12 Environmental Sensor Communication System Using eSim

1. Theory

SDI-12 (Serial Digital Interface at 1200 Baud) is an asynchronous, ASCII-based serial communications protocol designed for intelligent environmental sensors. The protocol specifies a half-duplex, single-wire transmission format operating at a bit rate of 1200 baud. Each character is transmitted as a 10-bit frame consisting of:

- 1 Start Bit – Logic 0 (Space)
- 7 Data Bits – ASCII payload, transmitted LSB first
- 1 Parity Bit – Even parity
- 1 Stop Bit – Logic 1 (Mark)

Experiment scope. This experiment focuses on the design, modelling, and circuit-level transient verification of the core SDI-12 Serializer and Frame Controller Engine using eSim. The timing core utilizes a 1200 Hz reference clock combined with a CD4017 decade counter to sequentially control ten bit-periods. Each bit period is approximately 833.3 µs. A master D flip-flop gates the clock through an ENABLE signal during frame transmission. A delayed reset mechanism associated with state Q9 ensures that the Stop bit is held for its full bit width without premature clipping, resulting in an accurate protocol-compliant digital serializer.

2. Schematic Diagram

The circuit schematic of the SDI-12 Serializer and Timing Controller implemented in eSim is shown below.

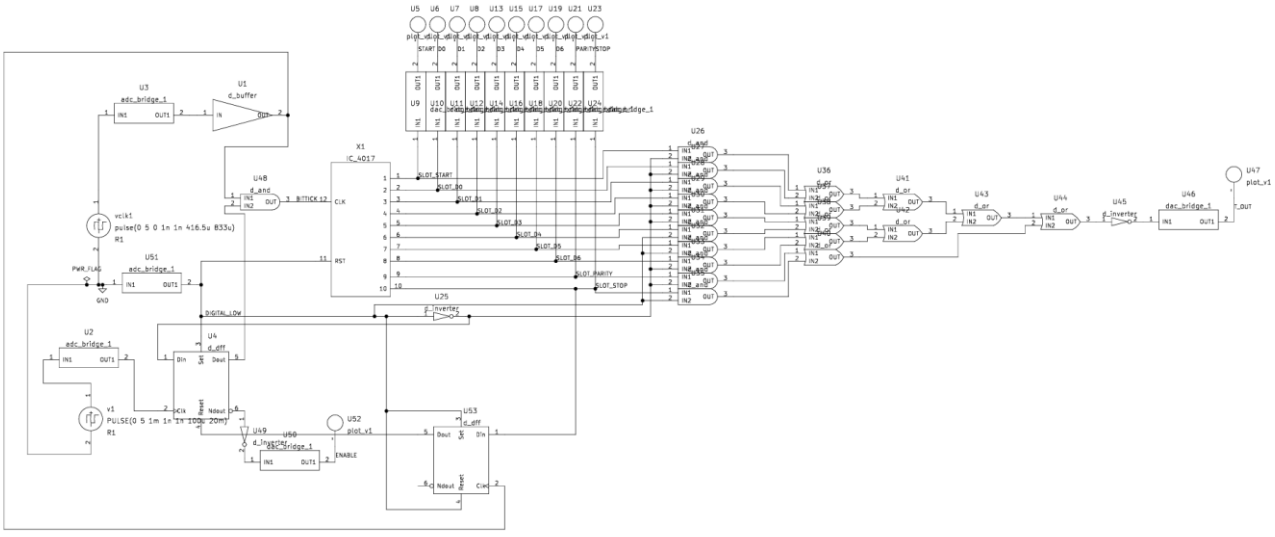

Figure 1: Circuit Schematic of the SDI-12 Communication Node Timing and Serializer Engine in eSim.

3. Simulation Results

3.1 Ngspice Plots

The transient simulation was performed using Ngspice to verify the timing controller, frame control signal, and serialized output waveform.

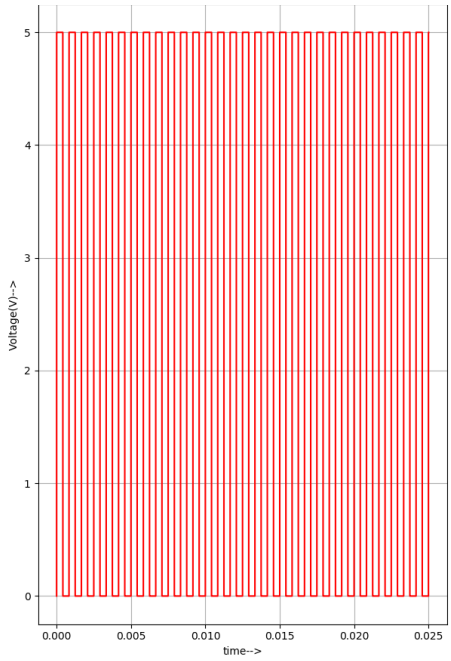

Figure 2: Ngspice Transient Analysis Plot showing the 1200 Hz Bit Clock (bittick)

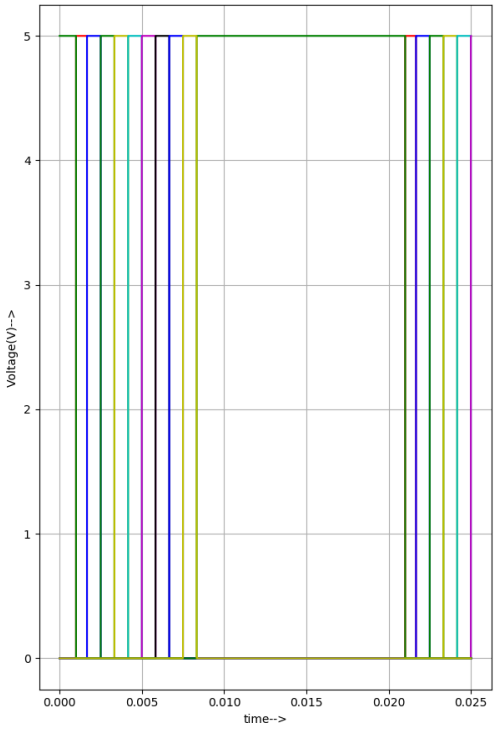

Figure 3: Ngspice simulation showing the 10 bits generated by the IC_4017

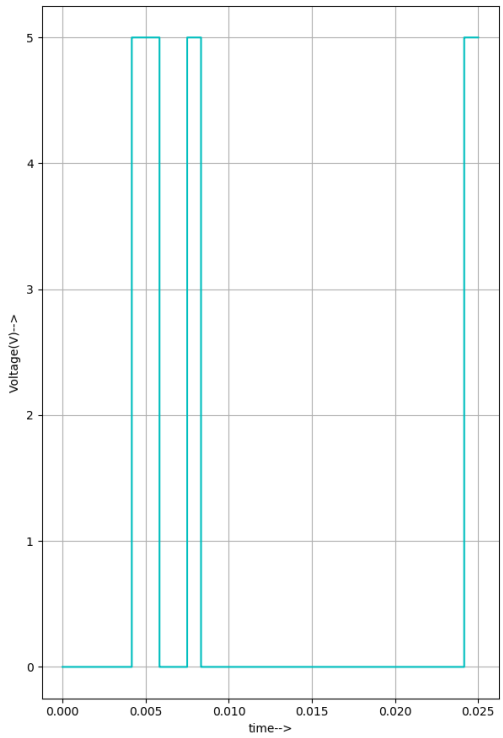

Figure 4: Ngspice simulation result showing the serialized output T_out with data "000110"

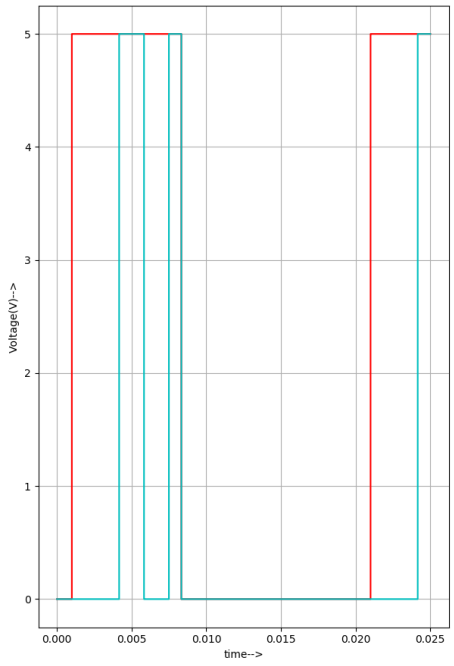

Figure 5: Ngspice Transient Analysis Plot showing the Frame Control (ENABLE), and Serialized Output (t_out).

3.2 Timing Verification

The 1200 Hz bit clock produces precise bit intervals of approximately 833.3 µs, corresponding to the required 1200-baud SDI-12 timing.

3.3 Frame Control Verification

The ENABLE signal transitions HIGH upon arrival of the TRIG_DIG signal and remains active for exactly ten bit periods, corresponding to approximately 8.33 ms, before returning to the 0 V idle state.

3.4 Data Transmission Verification

The serialized output waveform (t_out) correctly transmits the Start, Data, Parity, and Stop sequence with clean and correctly timed logic transitions. The waveform therefore demonstrates the intended operation of the serializer and frame timing engine.

4. Implementation Scope and System Deliverables

The following subsystems have been completed and verified through circuit-level simulation in eSim:

- **1200 Hz Clock Generator:** Provides the precise bit-tick reference required for standard 1200-baud SDI-12 framing.
- **CD4017 Decade Counter Timing Core:** Manages sequential progression through the ten frame states, Q0 through Q9.
- **Command and Frame Controller:** Uses synchronized D flip-flop logic to regulate clock gating and the duration of each frame.
- **Serializer Core:** Uses an AND/OR multiplexing structure to place the parallel character bits onto the single serialized output line, t_out.

5. Planned Extensions (Phase 2 / Future Roadmap)

Building upon the completed core transmitter and timing controller, the complete SDI-12 system architecture encompasses the following proposed scope items:

1. **Shared SDI-12 Communication Line & PHY Transceiver:** Circuit-level single-wire electrical connection and signal transfer with open-drain tri-state drivers.
2. **Data Recorder / Master Subsystem:** Integration of command generation, transmitter, and receiver units for master-driven communication.
3. **Sensor Node Receiver Core:** Implementation of a Break and Marking pulse detector (12 ms pulse validation) for waking up addressable sensor nodes.
4. **Command Reception & Decoding Engine:** Support for standard SDI-12 protocol command decoding:
    - Acknowledge Active Command (a!)
    - Start Measurement Command (aM!)
    - Data Request Command (aD0!)

5. **Measurement Data Transfer & Response Generation:** Automated sensor response transmission returning requested measurement payload data back to the Data Recorder.

6. Conclusion

Thus, the core timing, framing, and transmission engine of an SDI-12 environmental sensor node has been designed, modelled, and verified using eSim. Transient simulation results confirm accurate ten-bit frame control, precise 833.3 µs bit-period synchronization, and stable idle-state behavior. The implemented architecture provides a circuit-level foundation for extending the design with an SDI-12 receiver, break detector, and bi-directional physical layer interface in the next phase of development.

7. References

1. SDI-12 Support Group, "SDI-12: A Serial-Digital Interface Standard for Microprocessor-Based Sensors," Version 1.4, January 2019. Available at: https://www.sdi-12.org/
2. FOSSEE, "eSim: An Open Source EDA Tool for Circuit Design, Simulation, Analysis and PCB Design," Indian Institute of Technology Bombay. Available at: https://esim.fossee.in/