DESIGN AND SIMULATION OF AN 8-BIT CMOS VERNIER DELAY-LINE TIME-TO-DIGITAL CONVERTER USING eSim

Introduction:

A Time-to-Digital Converter (TDC) is a circuit that measures the time interval between two events, a START edge and a STOP edge, and converts that interval into a digital code. TDCs form a key building block in applications such as LIDAR ranging, particle-physics timing systems, and all-digital phase-locked loops, where sub-nanosecond timing resolution is required. A simple delay-line TDC obtains this resolution from the propagation delay of a single chain of logic gates, so making the resolution finer means adding more stages, which quickly becomes impractical. The Vernier delay-line technique overcomes this limitation by running two delay chains of slightly different speed, a slow path and a fast path, in parallel, so that the timing resolution is set by the small difference between the two delays rather than by the delay of an individual stage. This project designs and simulates an 8-bit CMOS Vernier Delay-Line TDC built from standard CMOS inverter delay cells and a transistor-level sampling arbiter, using eSim to verify the timing behaviour of the circuit before it is taken to layout.

Schematic Diagram:

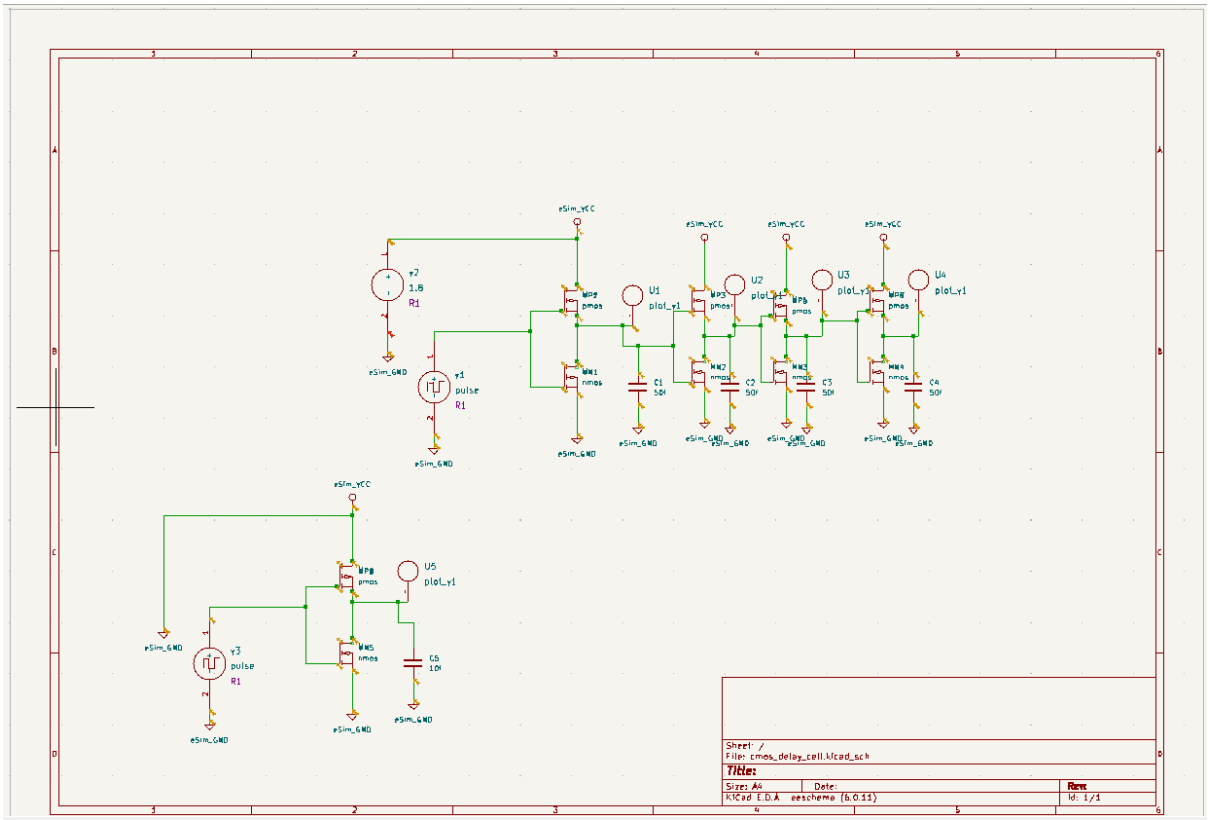

Fig. 1 — Slow-path (4-stage) and fast-path (1-stage) CMOS delay-cell schematic

NGSPICE Output waveform at output terminal:

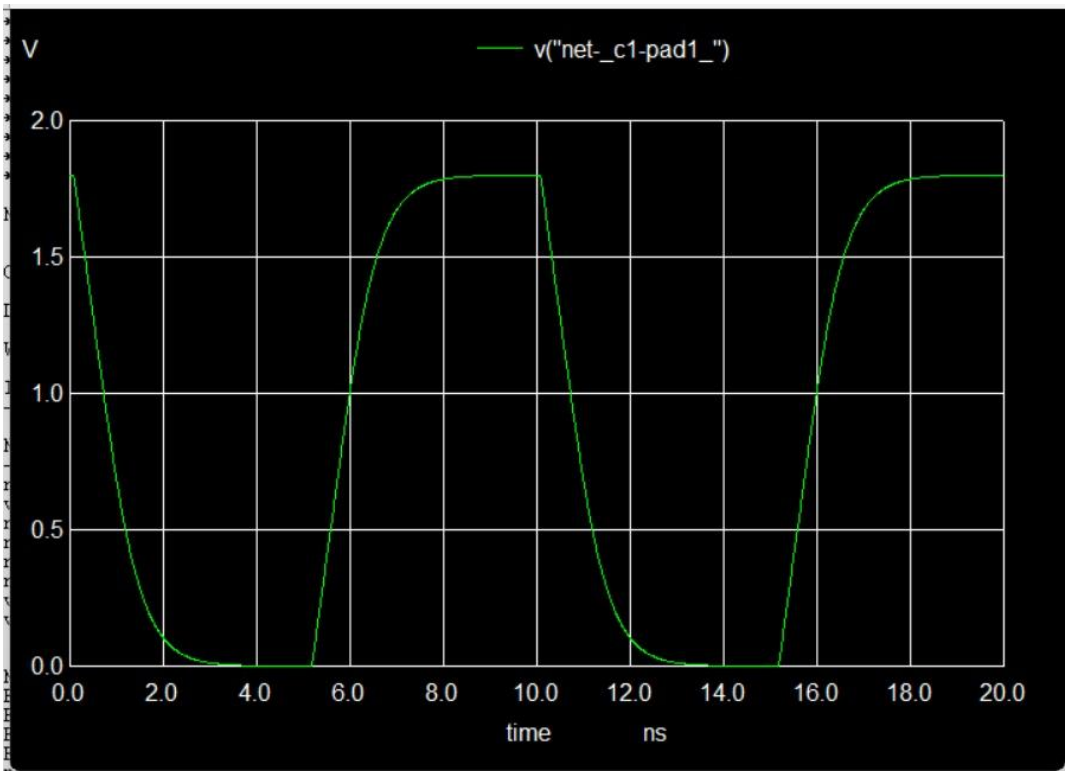

Fig. 2 — Output waveform of the 1st CMOS delay-cell stage (node net-*c1-pad1*)

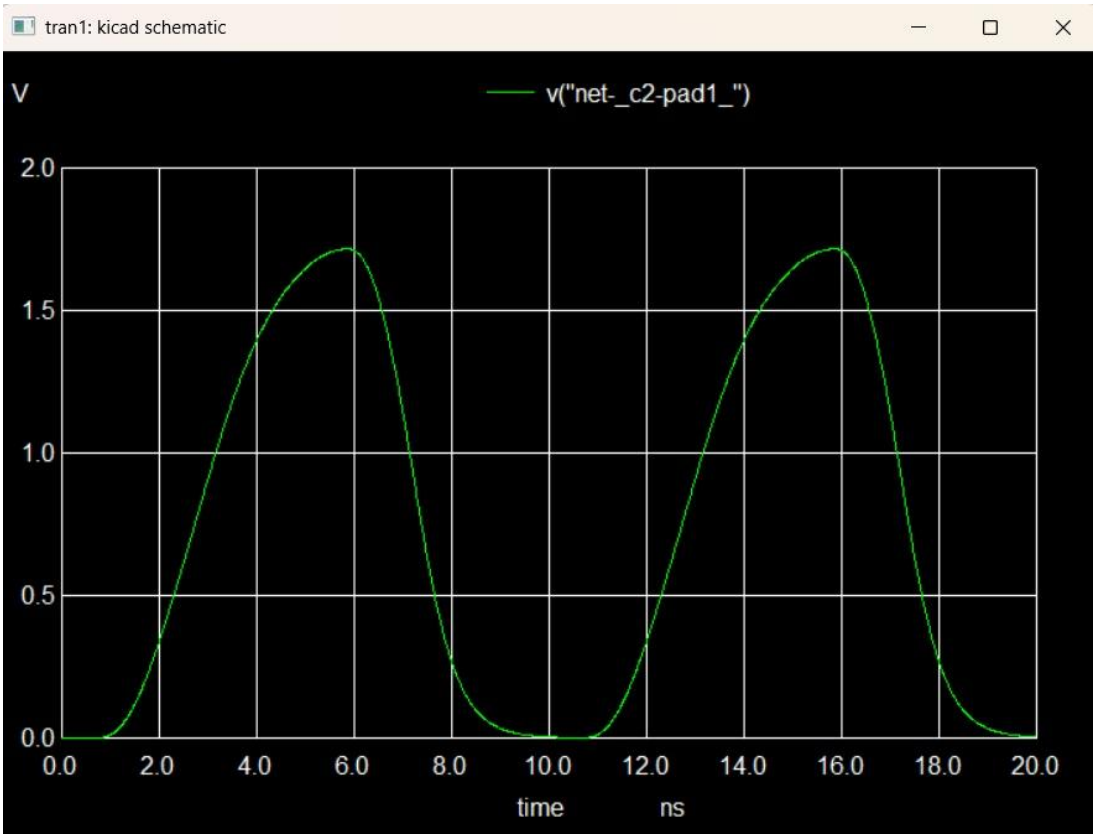

Fig. 3— Output waveform of the 2nd CMOS delay-cell stage (node net-*c2-pad1*)

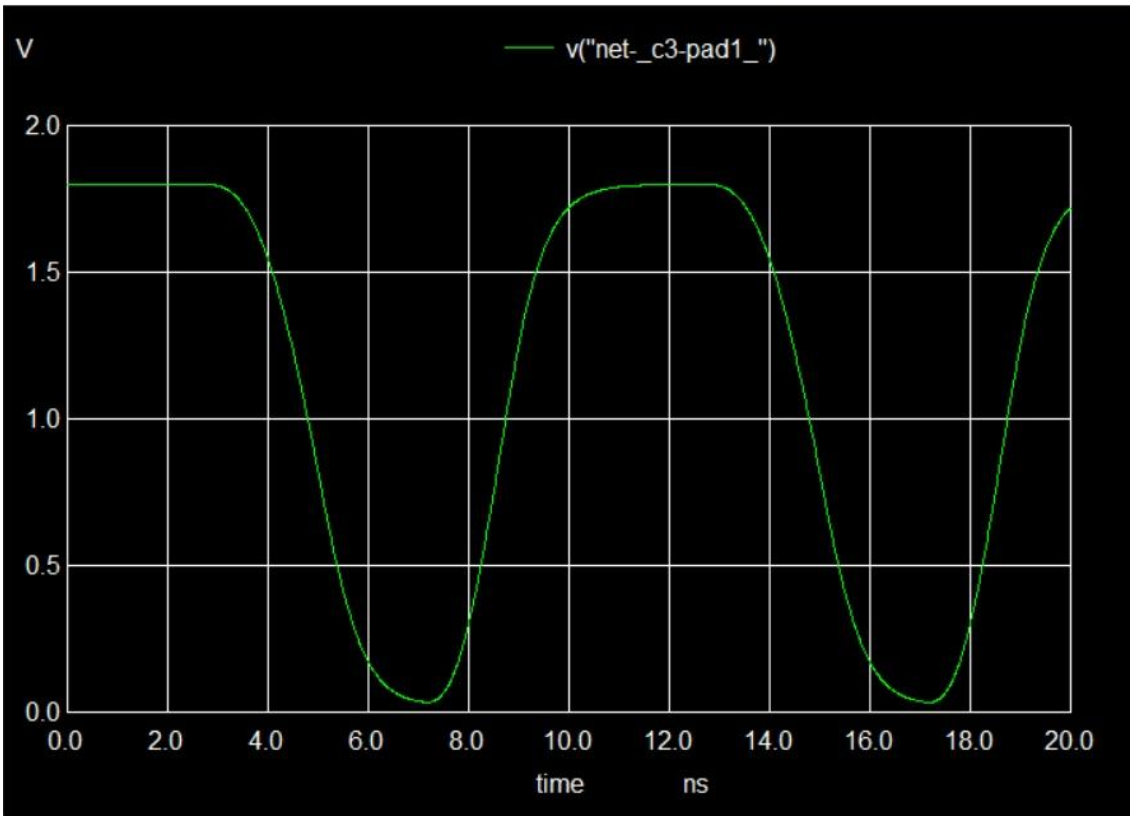

Fig. 4— Output waveform of the 3 rd CMOS delay-cell stage (node net-*c3-pad1*)

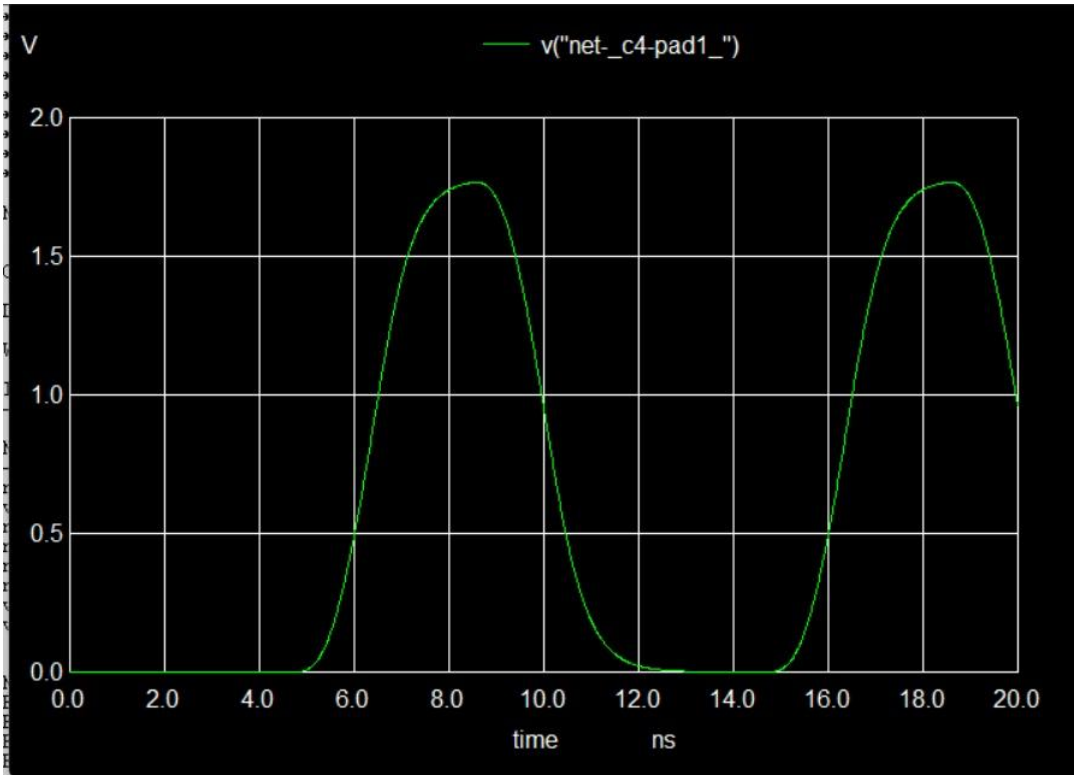

Fig. 5— Output waveform of the 4th CMOS delay-cell stage (node net-*c4-pad1*)

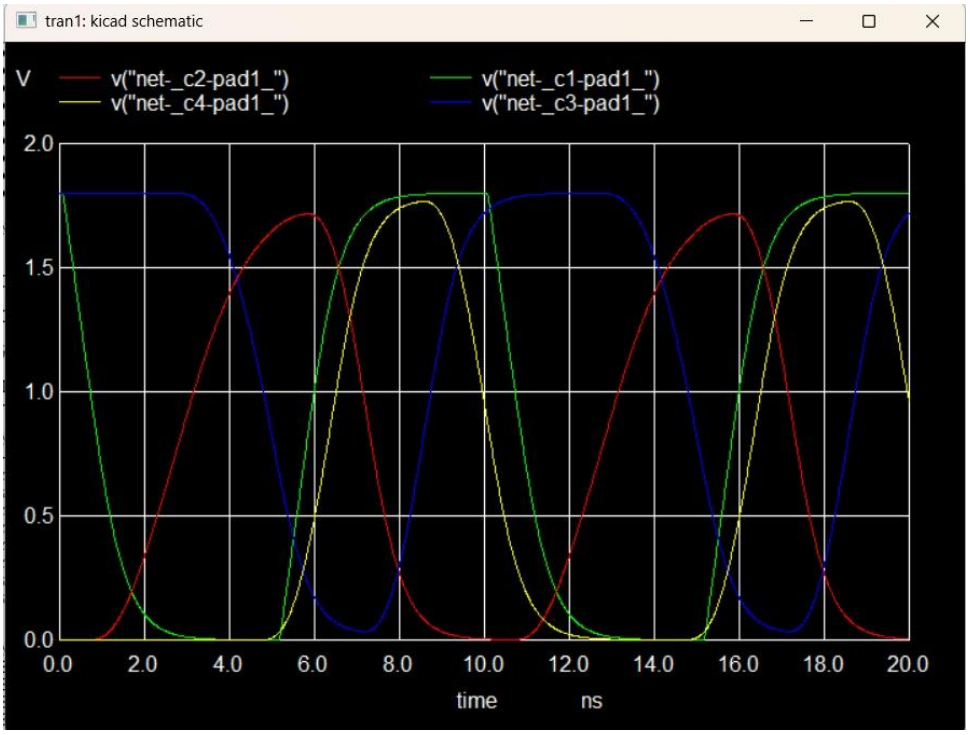

Fig. 6 — Combined output waveforms of the 4-stage slow delay chain (nodes net-*c1-pad1* to net-*c4-pad1*)

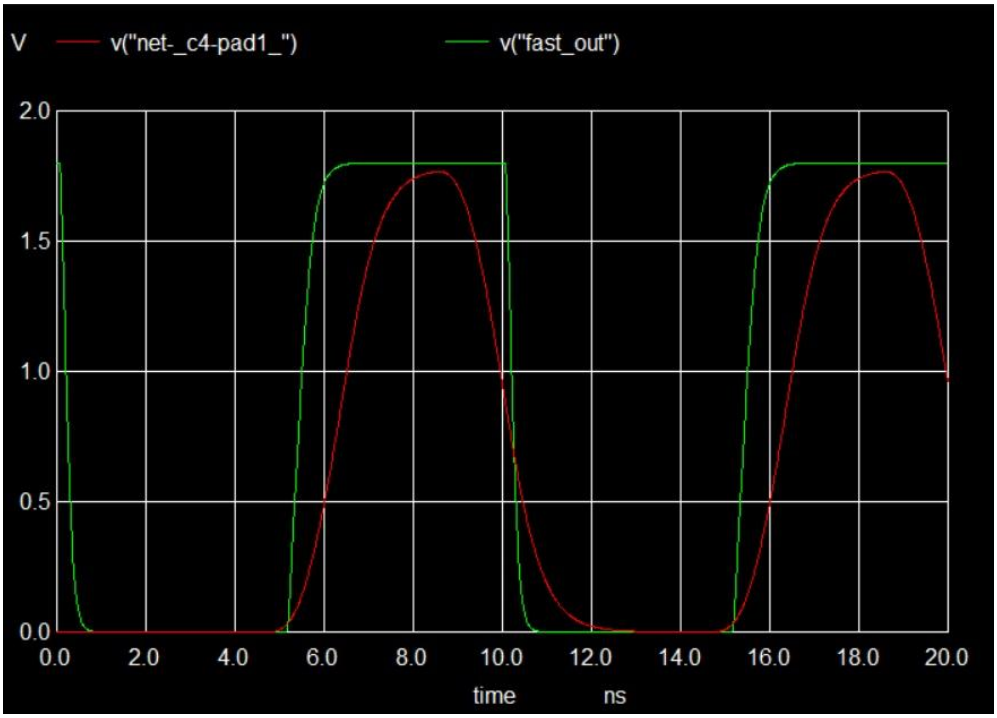

Fig. 7 — Comparison of fast-path output (fast_out) and slow-path output (net-*c4-pad1*), showing the timing offset Δτ between the two paths

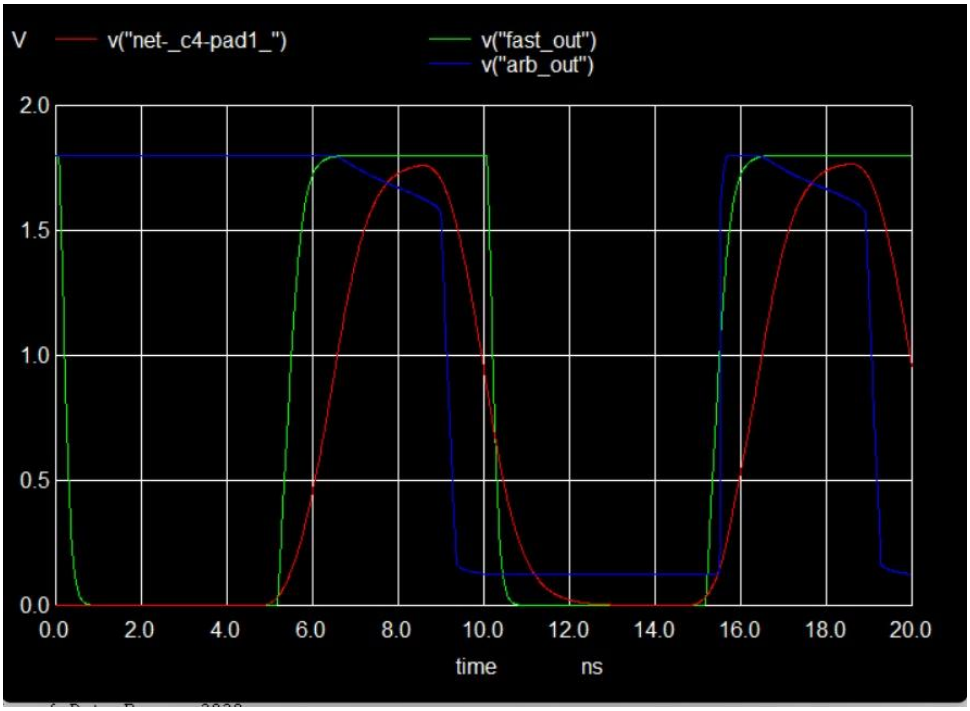

Fig. 8— Arbiter output (arb_out) relative to the fast-path and slow-path signals, showing the sampled timing decision

Python plots :

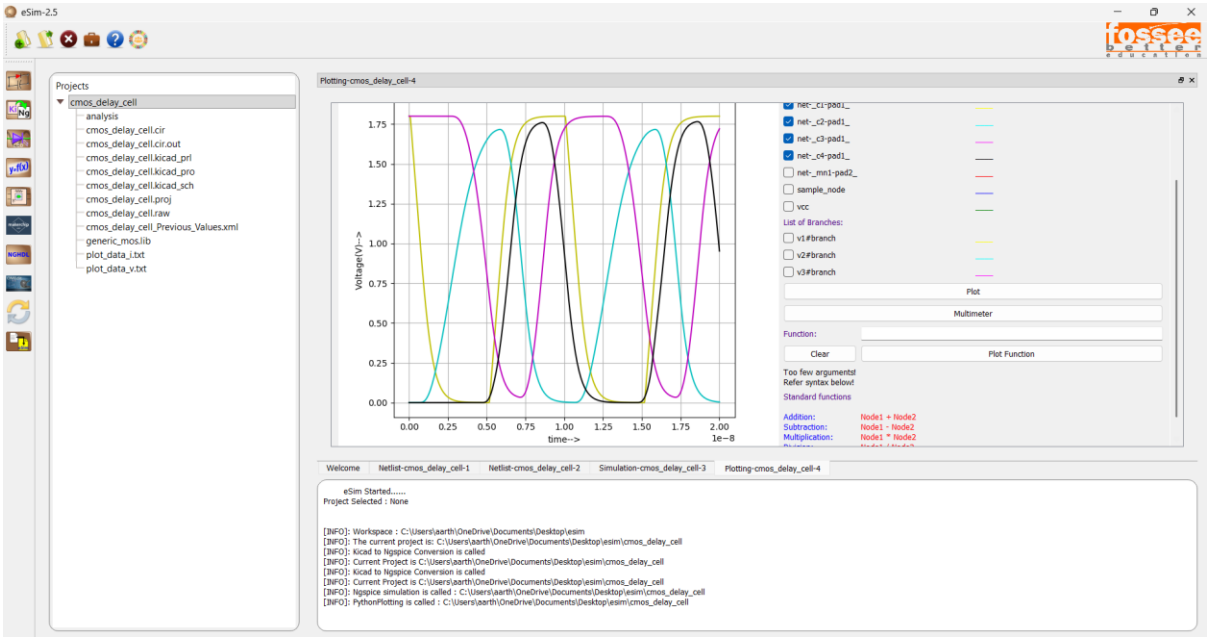

Fig. 9— eSim Python Plotting window showing the overlaid 4-stage slow delay chain outputs (net-*c1-pad1* to net-*c4-pad1*)

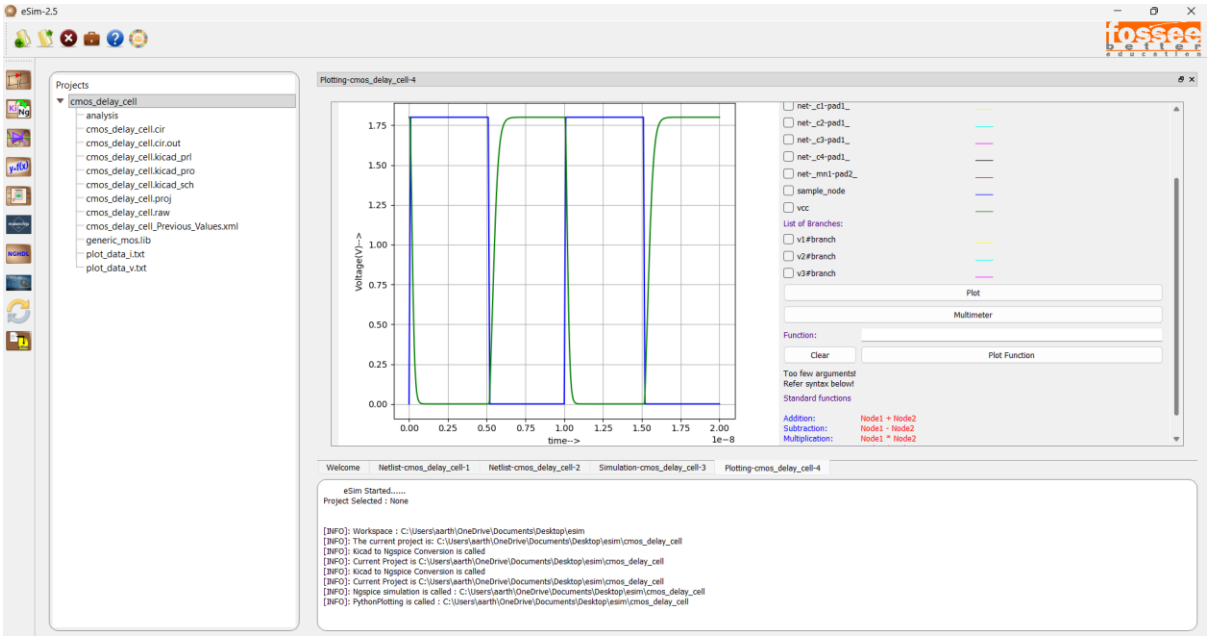

Fig. 10— eSim Python Plotting window showing the fast-path input and output waveforms (fast_in vs. fast_out)

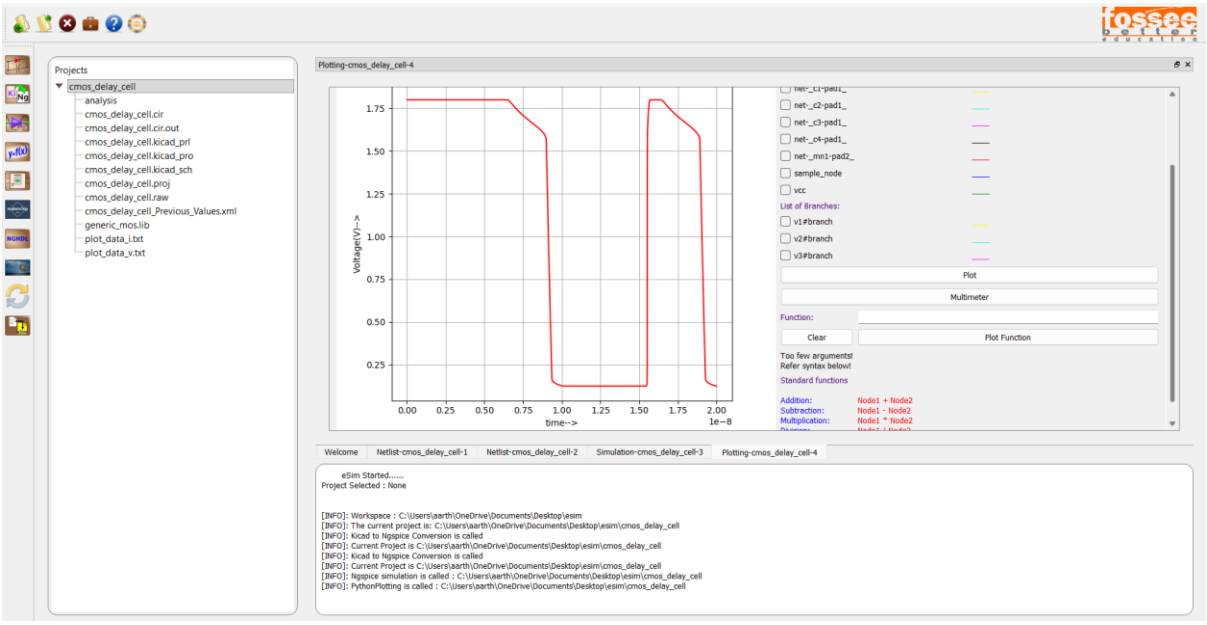

Fig. 11 — eSim Python Plotting window showing the arbiter output waveform (arb_out)

Reference:

1. eSim official documentation and user manual — https://esim.fossee.in/
2. NgSpice user manual — http://ngspice.sourceforge.net/docs.html
3. KiCad documentation — https://www.kicad.org/
4. N. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective* (for CMOS inverter propagation delay theory and Level-1 MOSFET model parameters)
5. P. Dudek, S. Szczepanski, and J. V. Hatfield, "A High-Resolution CMOS Time-to-Digital Converter Utilizing a Vernier Delay Line," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 2, pp. 240–247, Feb. 2000, DOI: 10.1109/4.823449

Conclusion:

Thus, an 8-bit CMOS Vernier Delay-Line Time-to-Digital Converter was designed and simulated using eSim. The transient simulation confirmed that the fast-path output switches noticeably earlier than the slow-path output, and that the sampling arbiter correctly captures the relative timing between the two paths to produce a stable digital decision output, validating the core Vernier TDC operating principle

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