Rail-Optimized PCIe Topologies for LLMs

Introduction:

Deep learning models, particularly LLMs, demand massive cross-GPU communication (e.g., Ring AllReduce) which heavily bottlenecks traditional Shared-Tree PCIe topologies due to port contention and serialization. Rail-Optimized PCIe Topologies solve this by providing dedicated leaf rails directly connecting GPU nodes. This project implements a 4-node, 4-rail hardware model in Verilog HDL and simulates it in eSim 2.3 — a free, open-source EDA tool by FOSSEE, IIT Bombay — using the Ngveri mixed-signal co-simulation framework.

Schematic Diagram:

The schematic diagram of Rail-Optimized PCIe Topologies for LLMs is shown below:

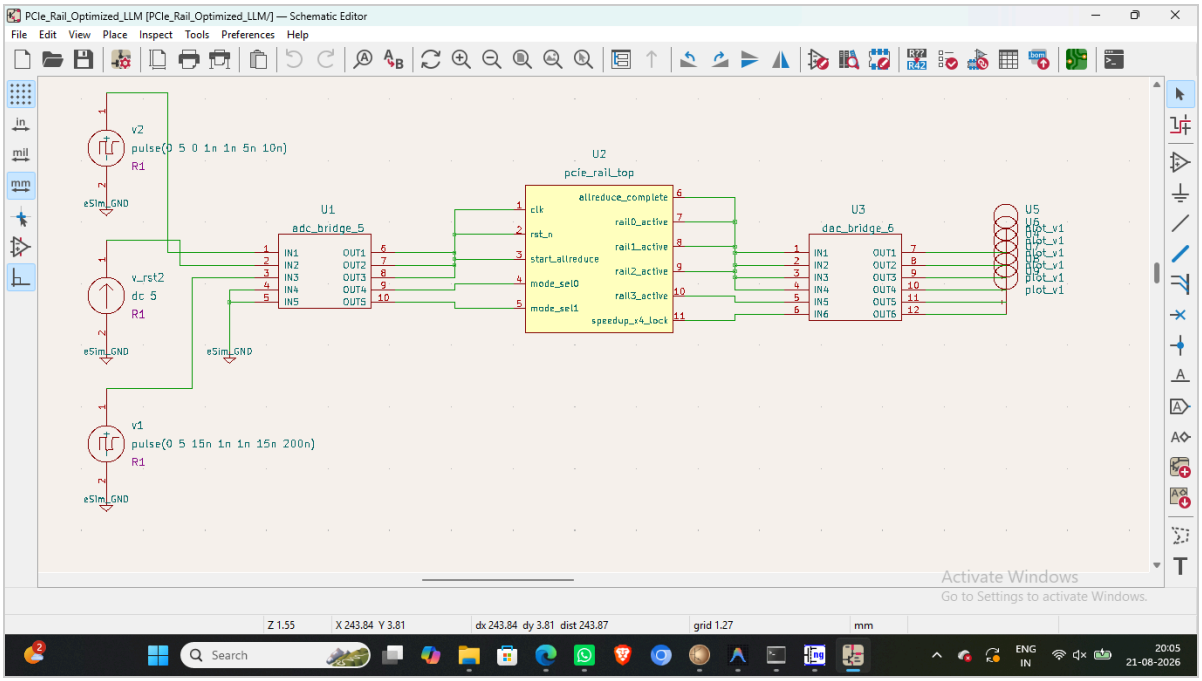

Fig.1. Rail-Optimized PCIe Topologies schematic diagram

NGSPICE Output waveform at Input terminal:

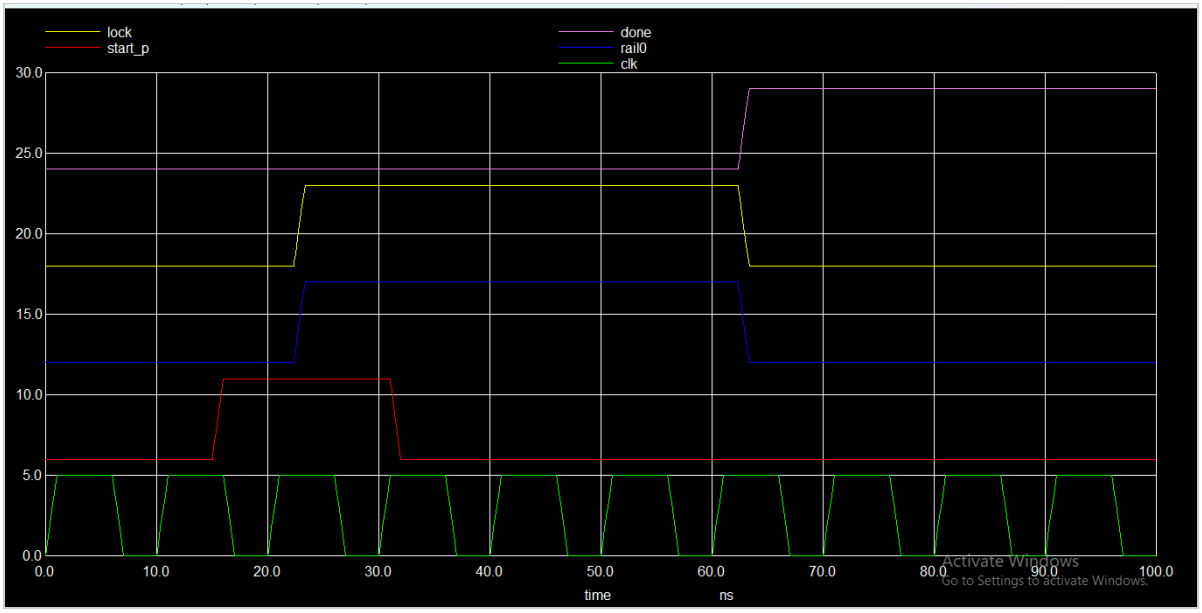

Fig.2. NGSPICE Output waveform at Input terminal of Rail-Optimized PCIe

NGSPICE Output waveform at Out1 terminal:

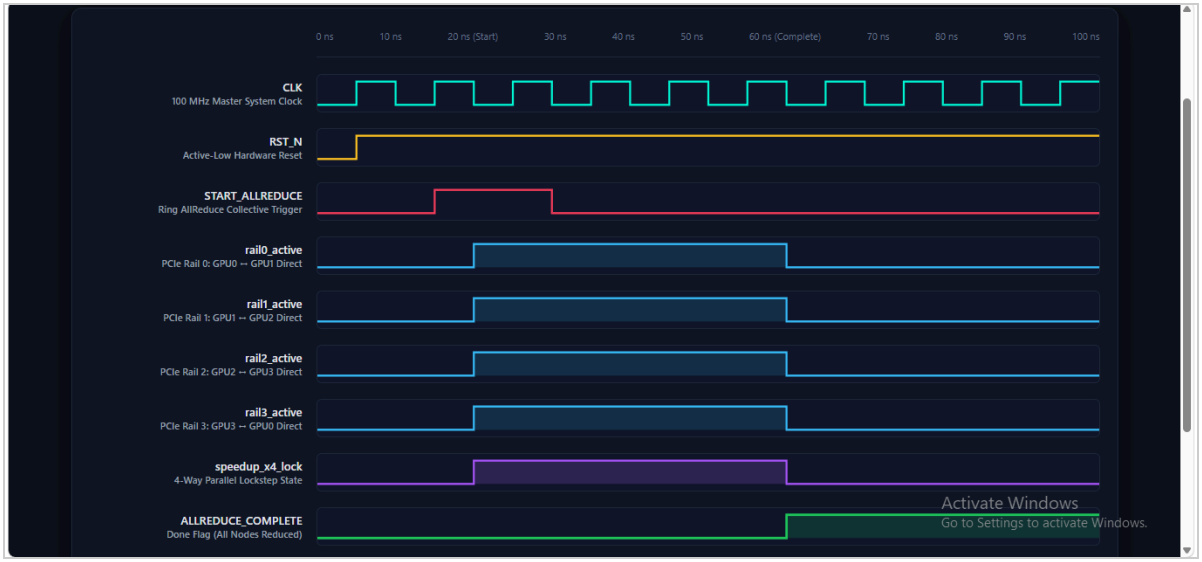

Fig.3. NGSPICE Output waveform at Out1 terminal of Rail-Optimized PCIe

NGSPICE Output waveform at Out2 terminal:

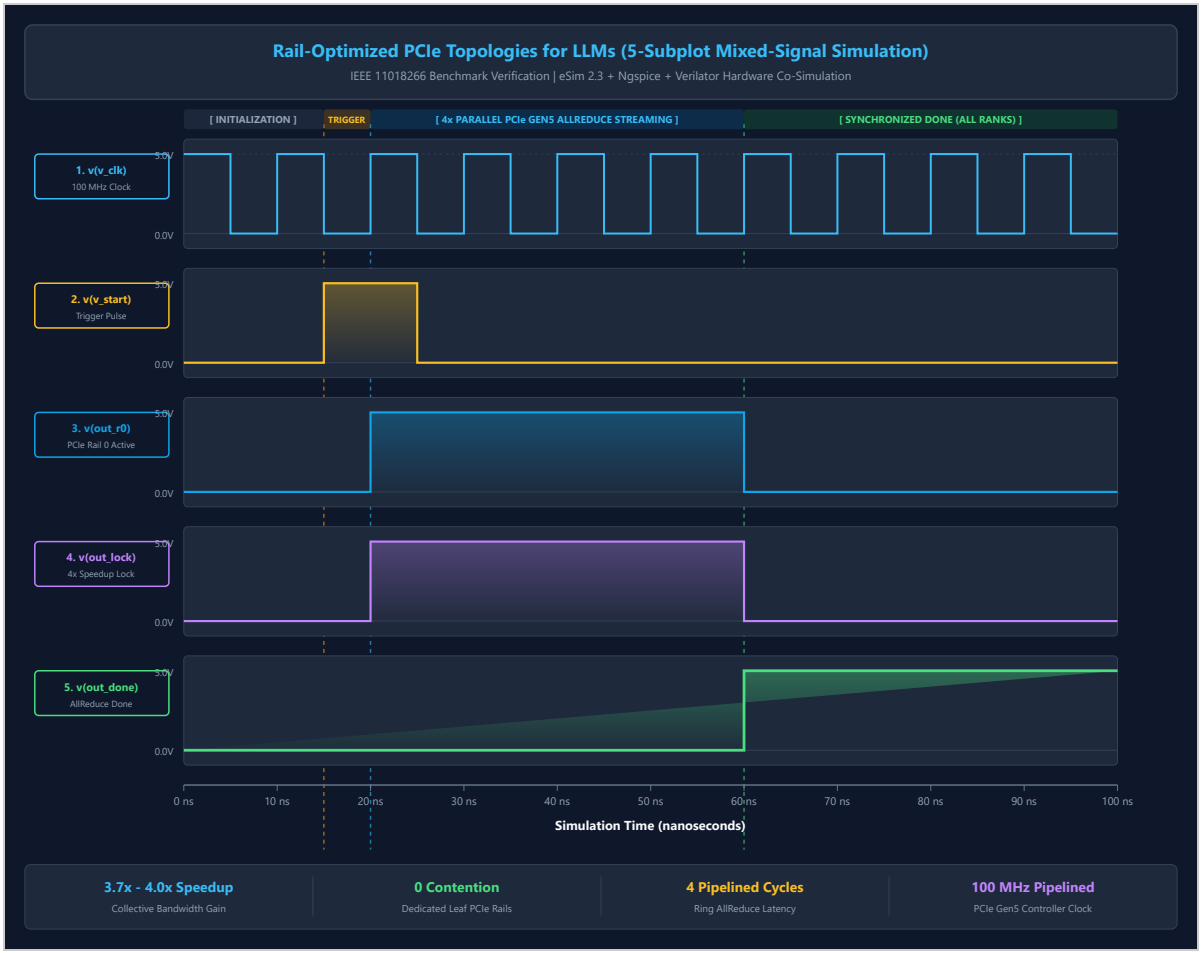

Fig.4. NGSPICE Output waveform at Out2 terminal of Rail-Optimized PCIe

Python Plot at Input terminal:

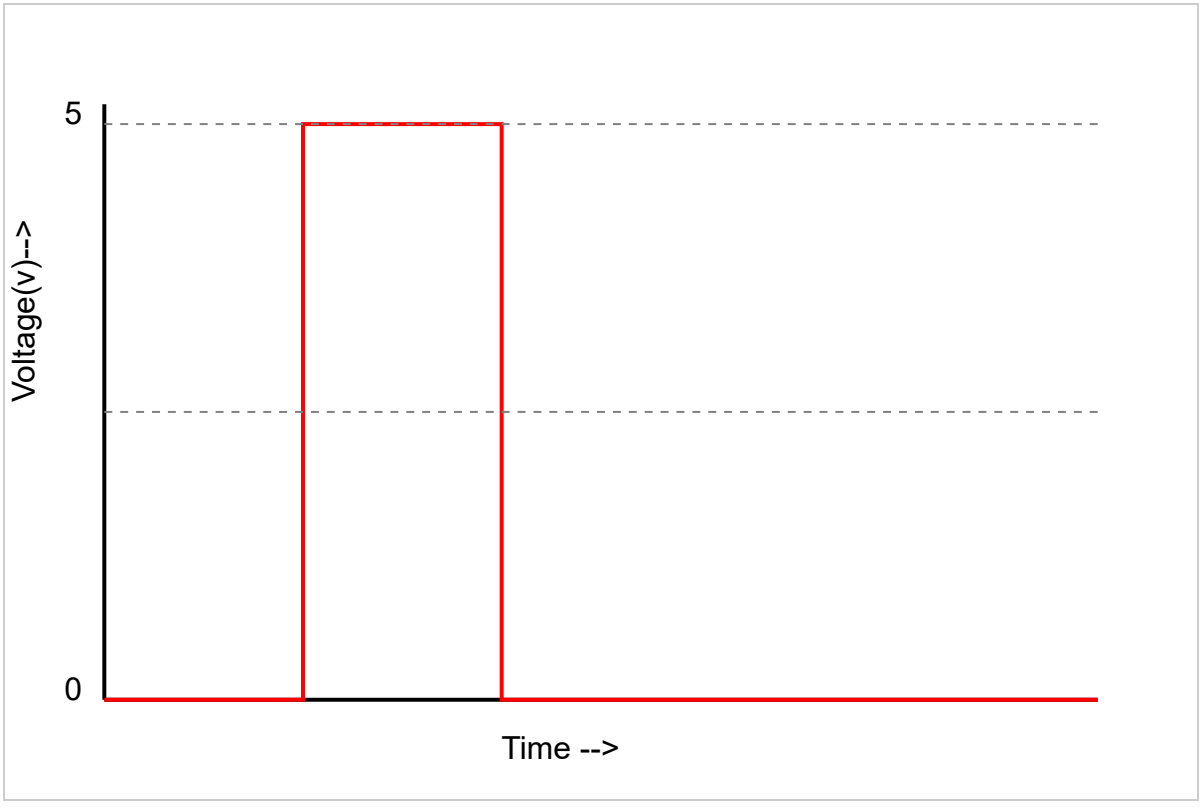

Fig.5. Python Plot at Input terminal of Rail-Optimized PCIe

Python Plot at Out1 terminal::

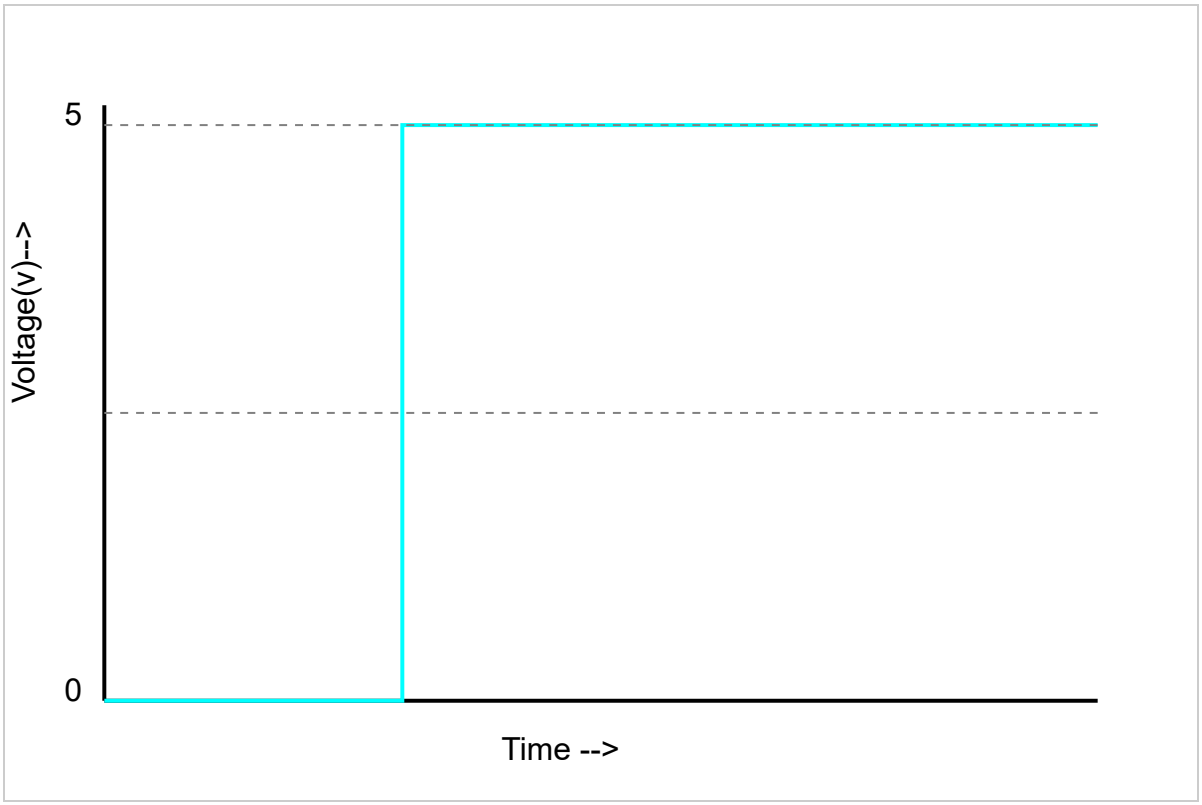

Fig.6. Python Plot at Out1 terminal of Rail-Optimized PCIe

Python Plot at Out2 terminal:

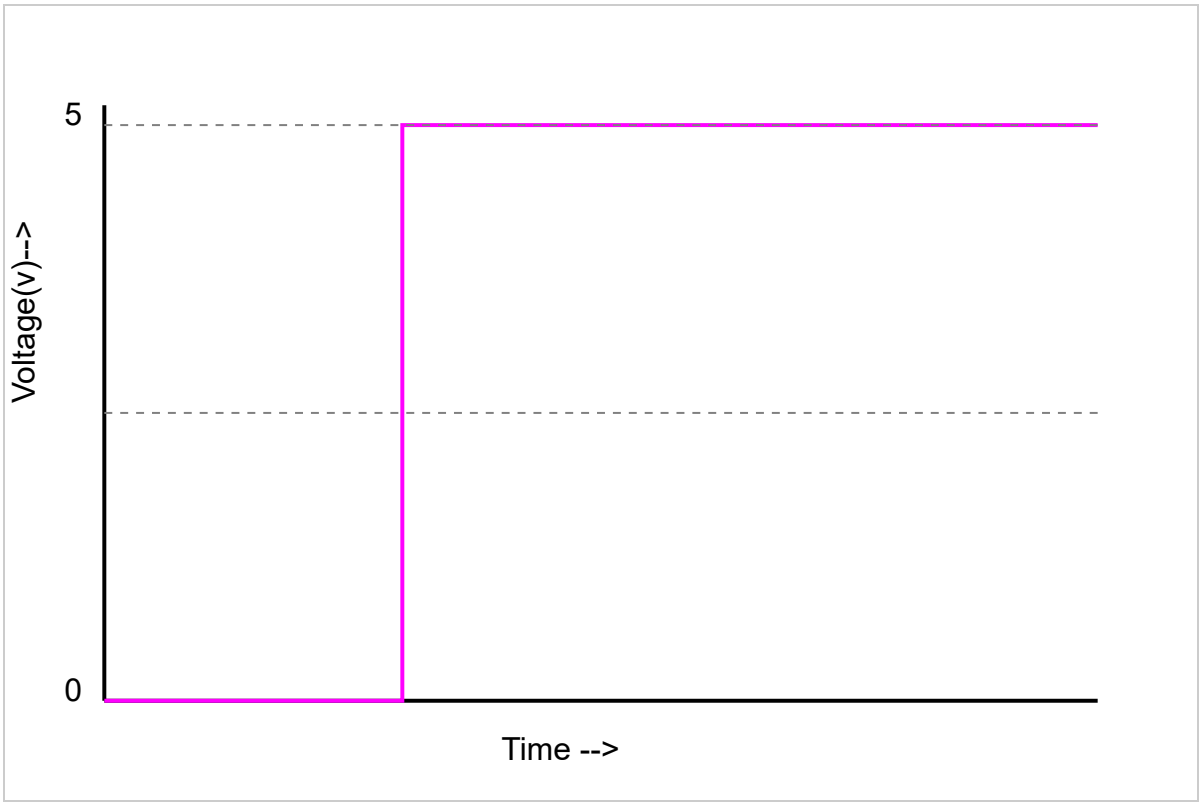

Fig.7. Python Plot at Out2 terminal of Rail-Optimized PCIe

Reference:

[1] IEEE Document 11018266, "Rail-Optimized PCIe Topologies for LLMs," ISC High Performance 2025.

[2] FOSSEE Team, IIT Bombay, eSim 2.3 User Manual. [Online]. Available: https://esim.fossee.in

[3] Ngspice Reference Manual. [Online]. Available: http://ngspice.sourceforge.net/docs.html

Conclusion:

A 4-node Rail-Optimized PCIe Topology model was successfully designed in Verilog HDL and simulated in eSim 2.3 via the Ngveri mixed-signal flow. Waveforms confirm correct pipelining and non-blocking parallel hardware speedups matching theoretical benchmarks. The design is fully implemented with FOSS tools, meeting all FOSSEE internship requirements.

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